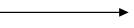
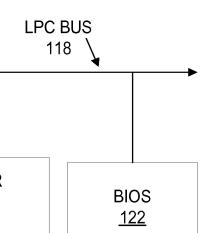


Fig. 1A (Prior Art)









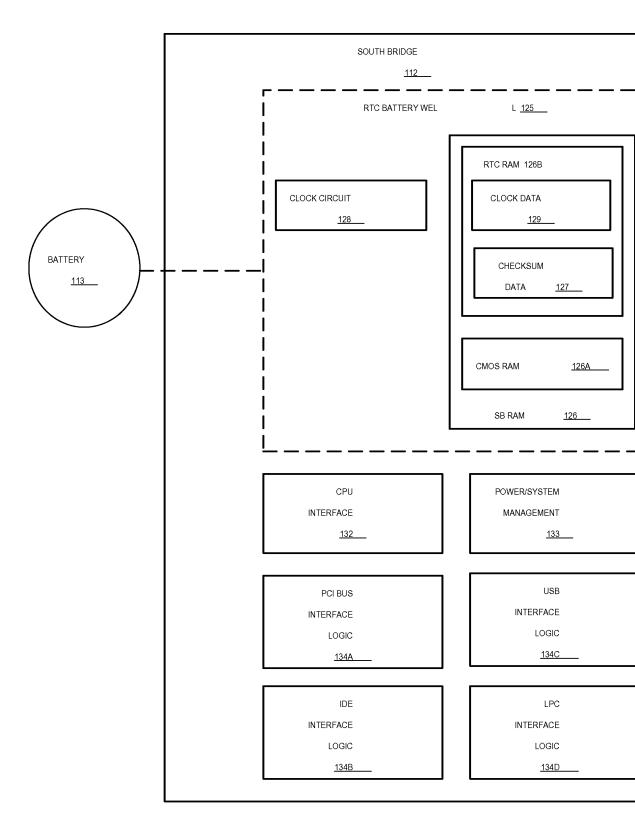


Fig. 1B (Prior Art)

	l
L <u>125</u>	
	] I
RTC RAM 126B	 
CLOCK DATA	] ]
<u>129</u>	 
CHECKSUM	
DATA <u>127</u>	
MOS RAM <u>126A</u>	   
SB RAM <u>126</u>	
POWER/SYSTEM	
MANAGEMENT	
<u>133</u>	
USB	
INTERFACE	
LOGIC	
<u>134C</u>	]
LPC	
INTERFACE	
LOGIC	
<u>134D</u>	
	-

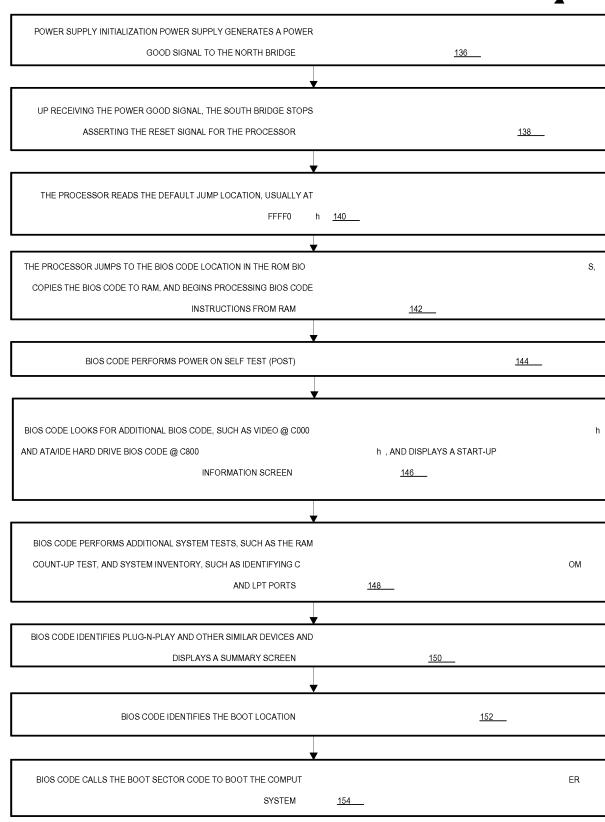


Fig. 2A (Prior Art)

	135
136	
<u>138</u>	
	S,
144	_ ]
A START-UP	h
	ОМ
_	
<u>152</u>	
	ER

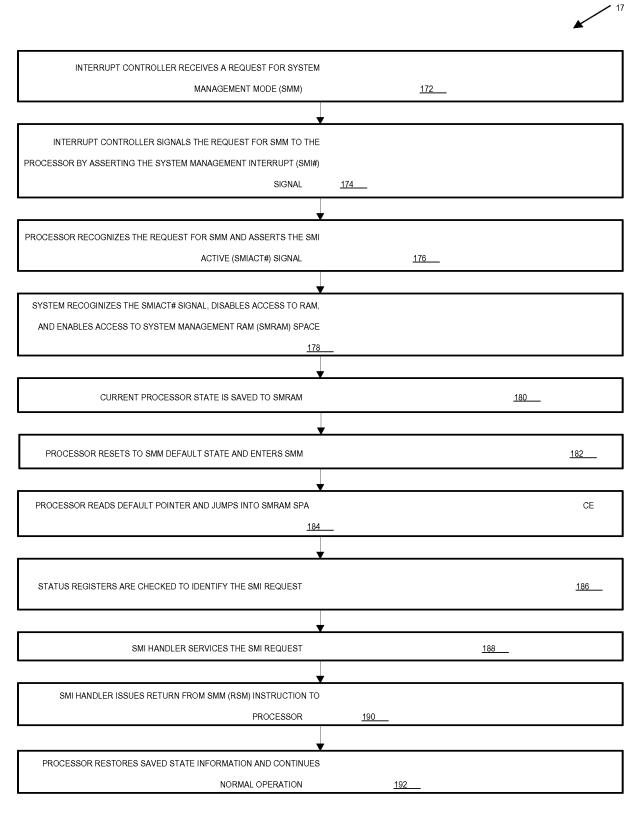


Fig. 2B (Prior Art)

	170
<u>180</u>	
	182
	CE
	<u>186</u>
<u>188</u>	

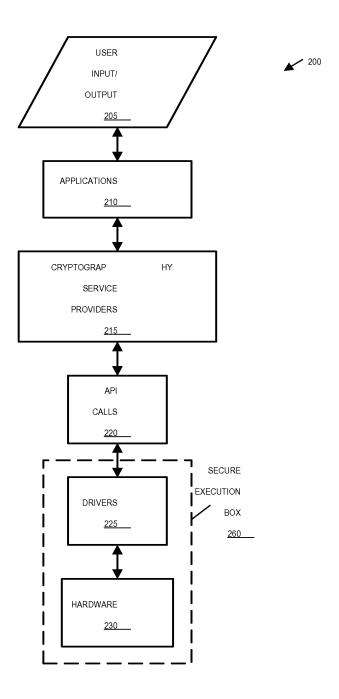
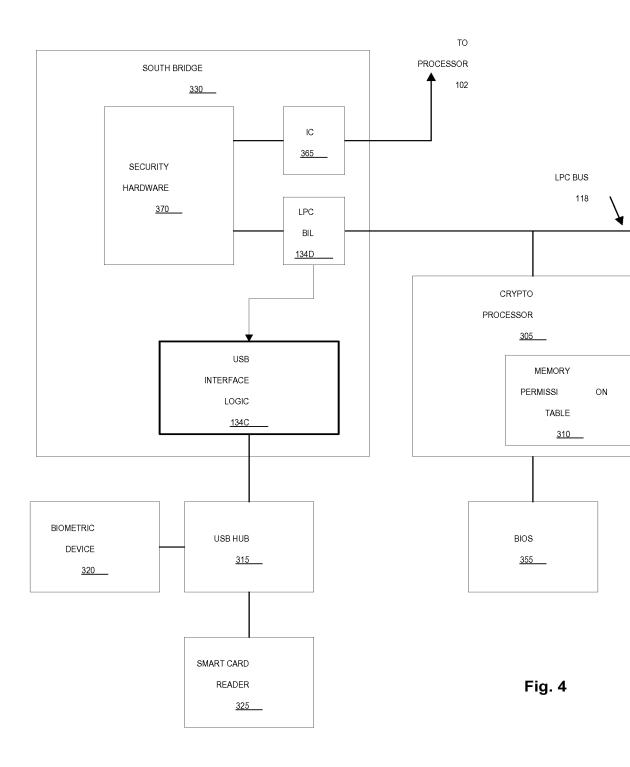


Fig. 3



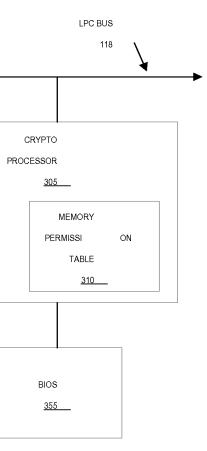


Fig. 4

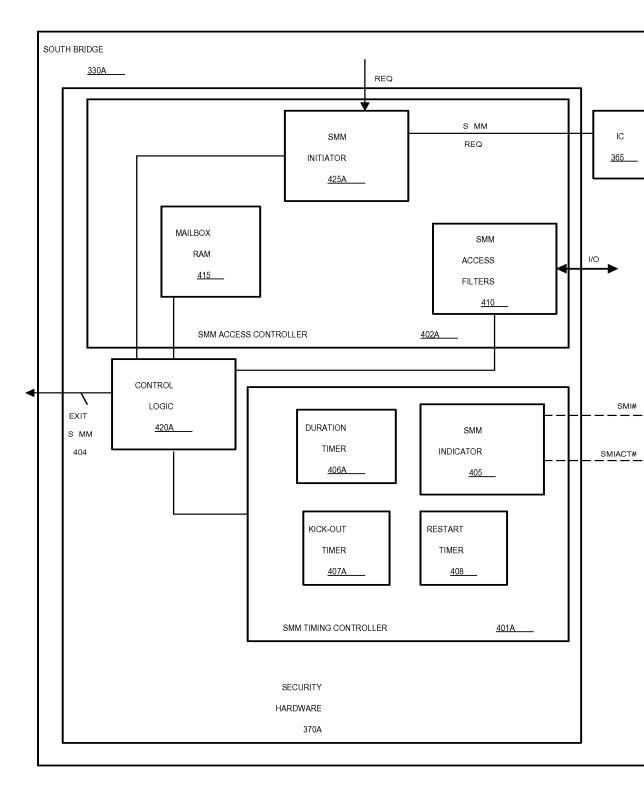
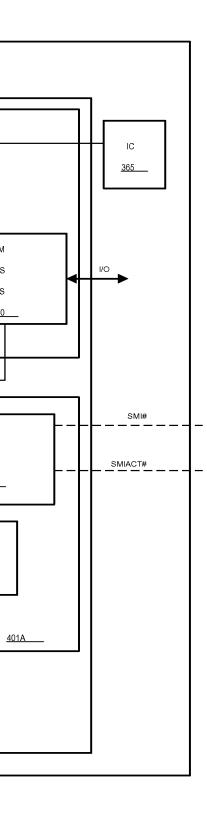


Fig. 5A



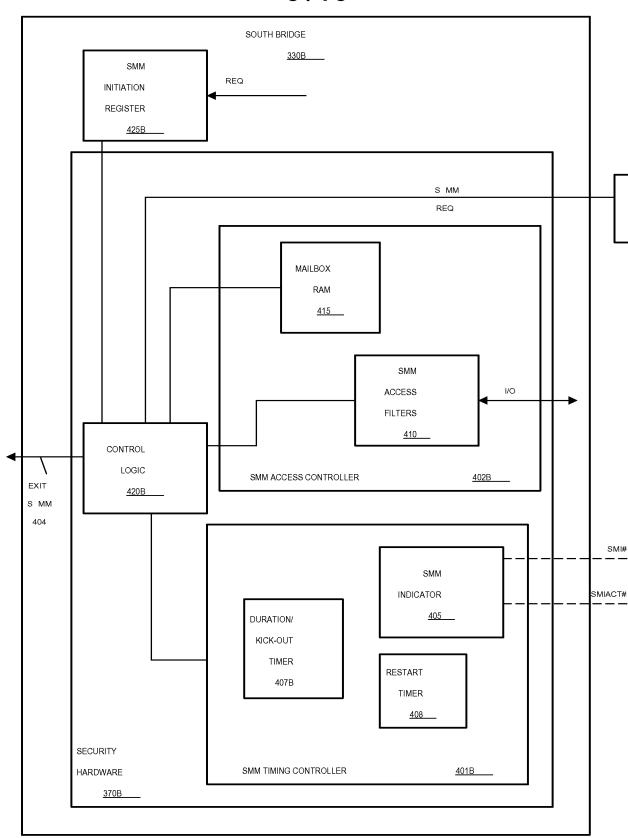
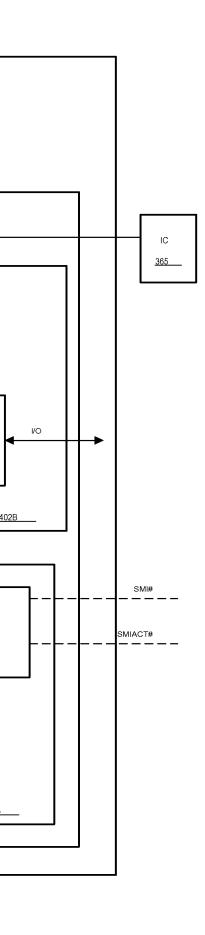


Fig. 5B



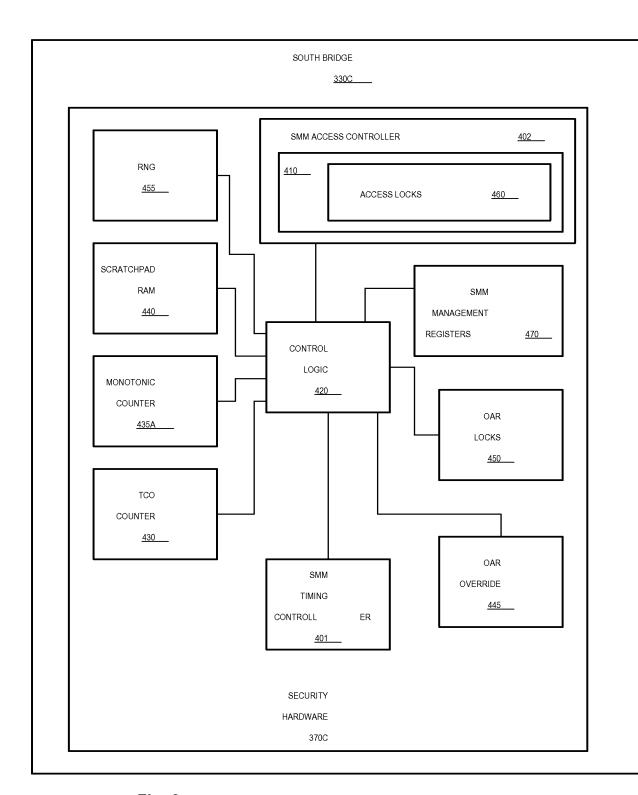
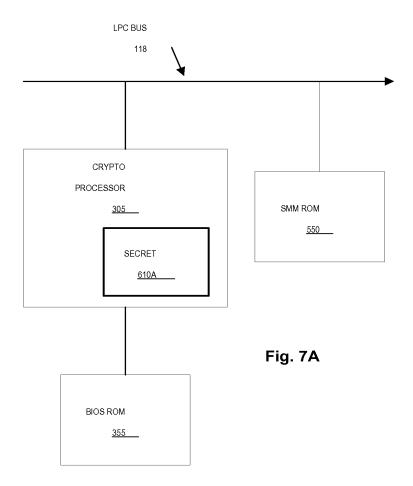


Fig. 6

402 <u>460</u> <u>470</u> OAR CKS 450 OAR RIDE 445



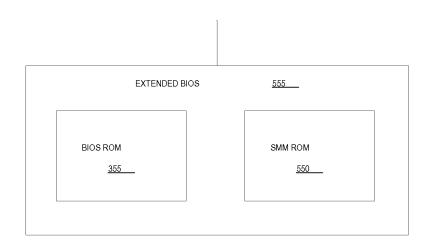


Fig. 7B

555\_\_\_\_\_SMM ROM

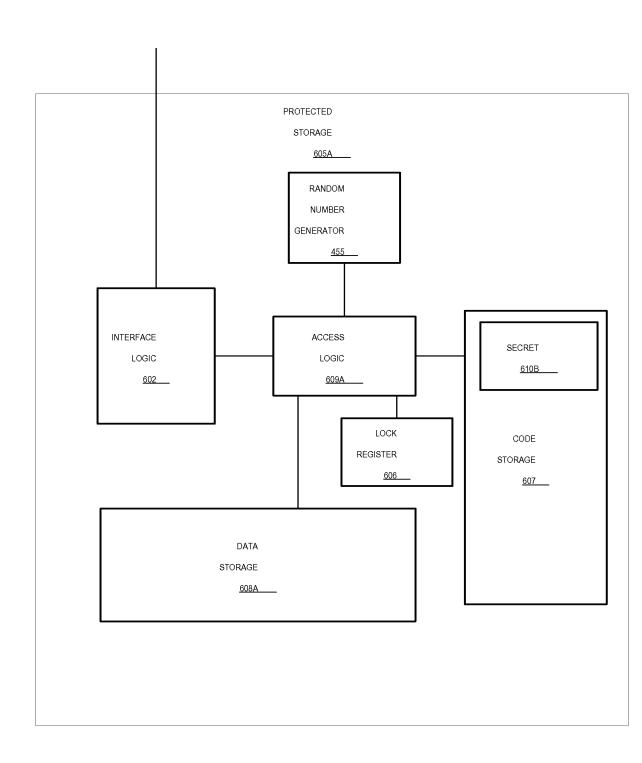


Fig. 7C

SECRET 610B

CODE STORAGE

607

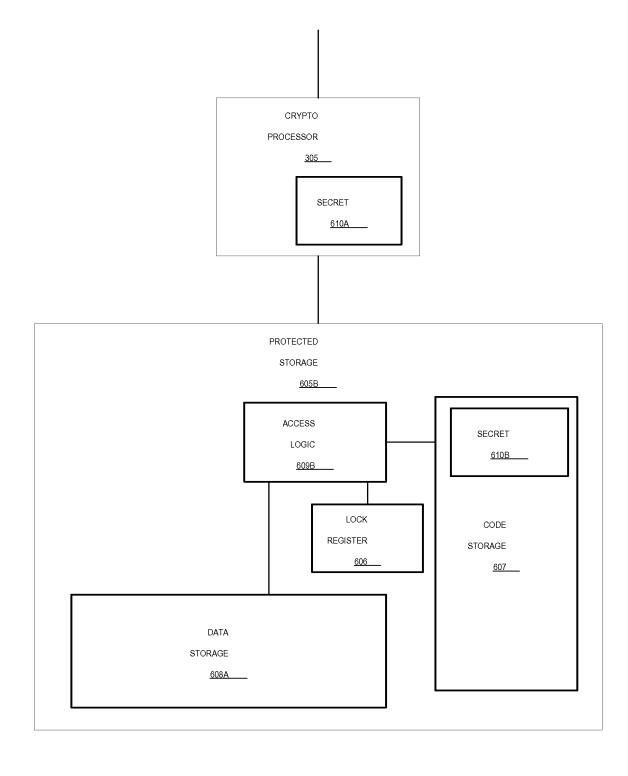


Fig. 7D

SECRET
610B

CODE
TORAGE
607

BIOS ROM					
<u>355</u>					
	DATA				
		608B			
	oroner.	DDWATE MENODY			
	SECRET 610C	PRIVATE MEMORY  606			

Fig. 8A

## 14 / 73

	SMM ROM
	<u>550                                   </u>
SECRET 610D	PUBLIC 0 625
SMM ROM 0 615	PUBLIC 1 630
SMM ROM 1 616	RESERVED 635
SMM ROM 2 617	REGISTERS 640
	MONOTONIC  COUNTER  435B

Fig. 8B

7		

## 15 / 73

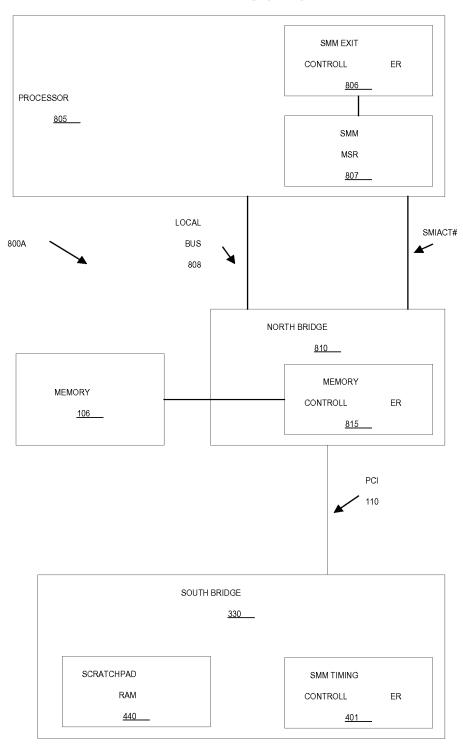


Fig. 9A

MIA(	CT#		

## 16 / 73

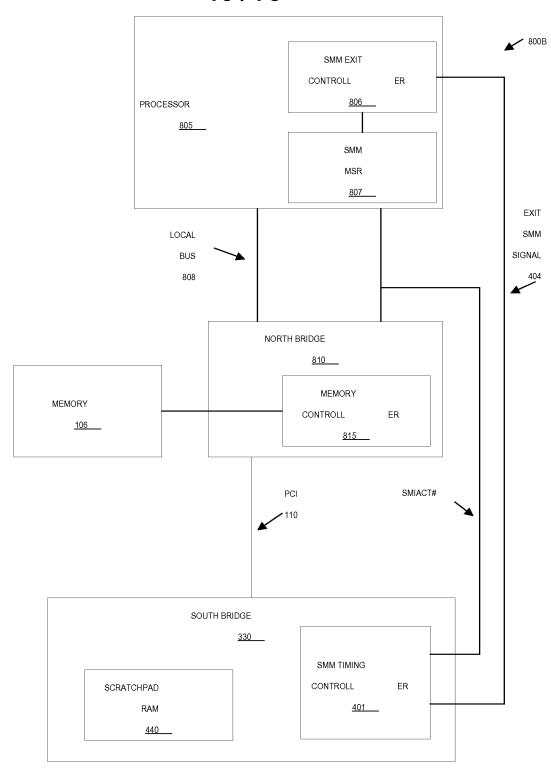
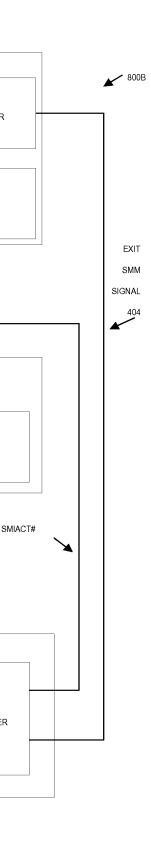


Fig. 9B



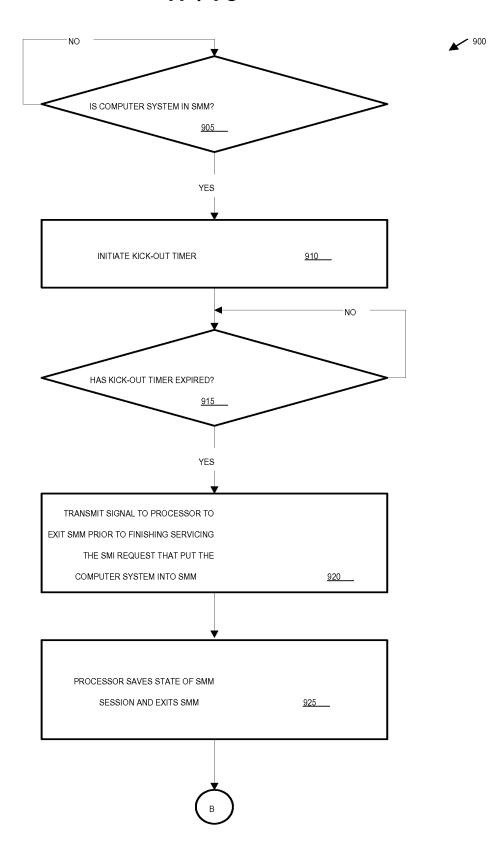


Fig. 10A

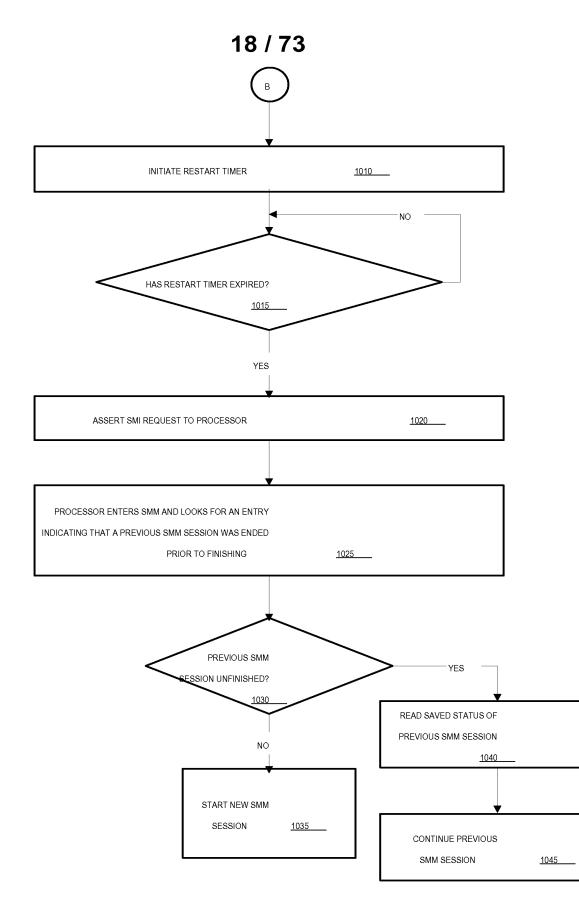
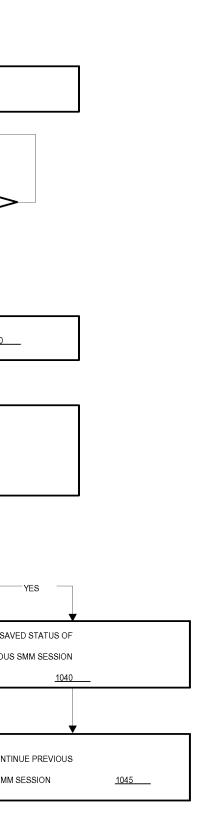


Fig. 10B



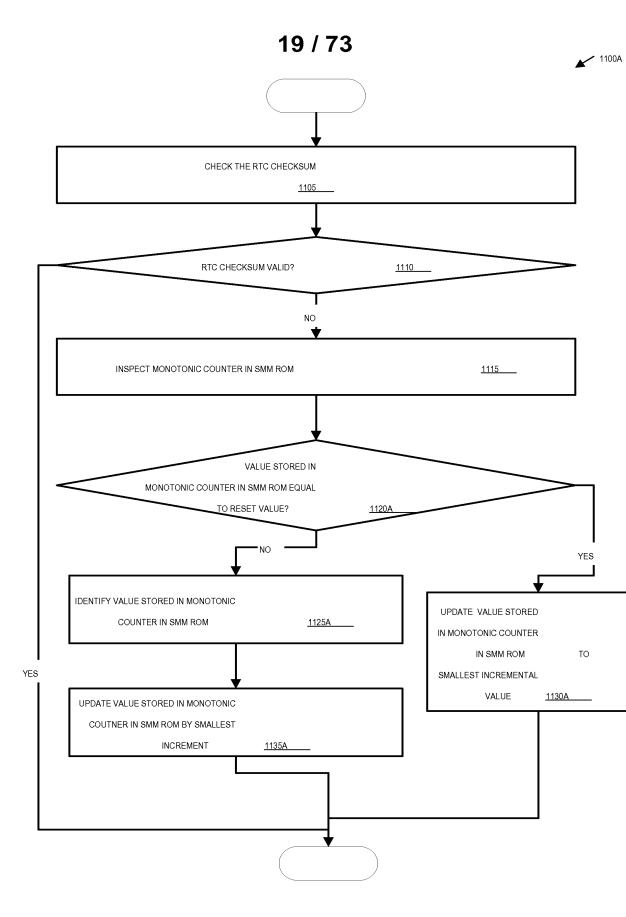
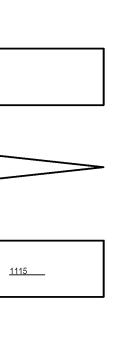
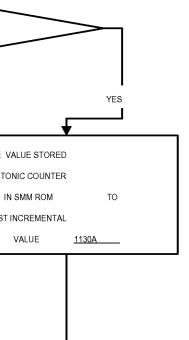


Fig. 11A





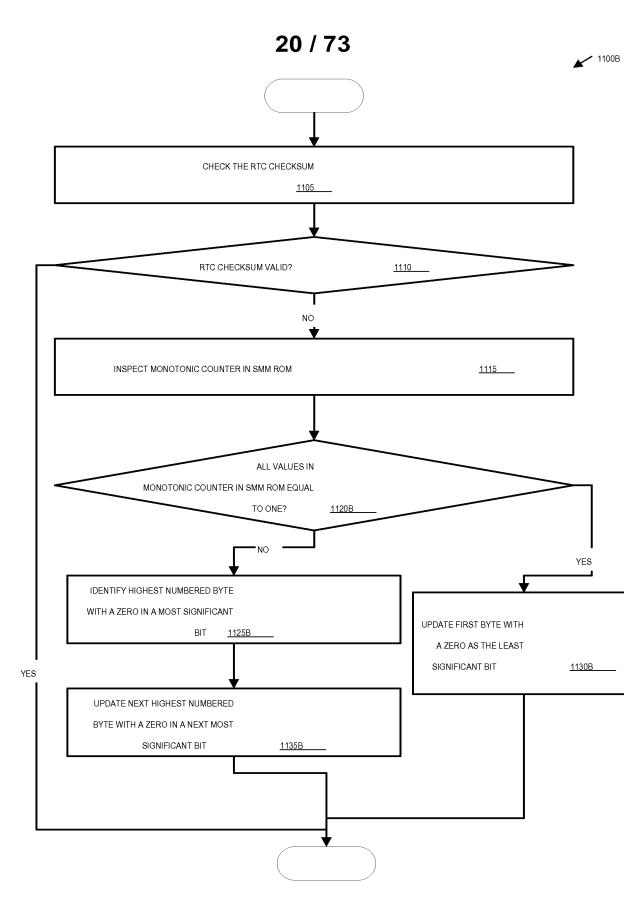
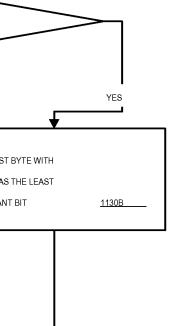


Fig. 11B

1115\_\_\_\_



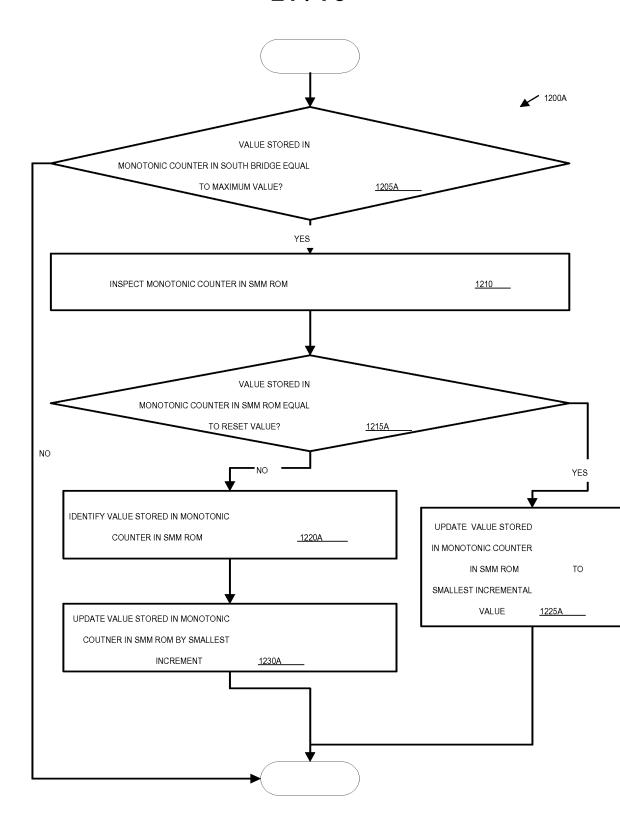
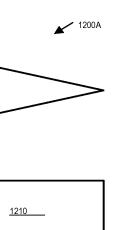
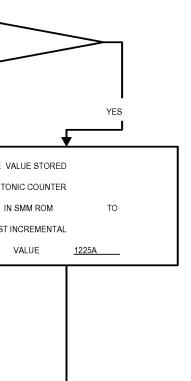


Fig. 12A





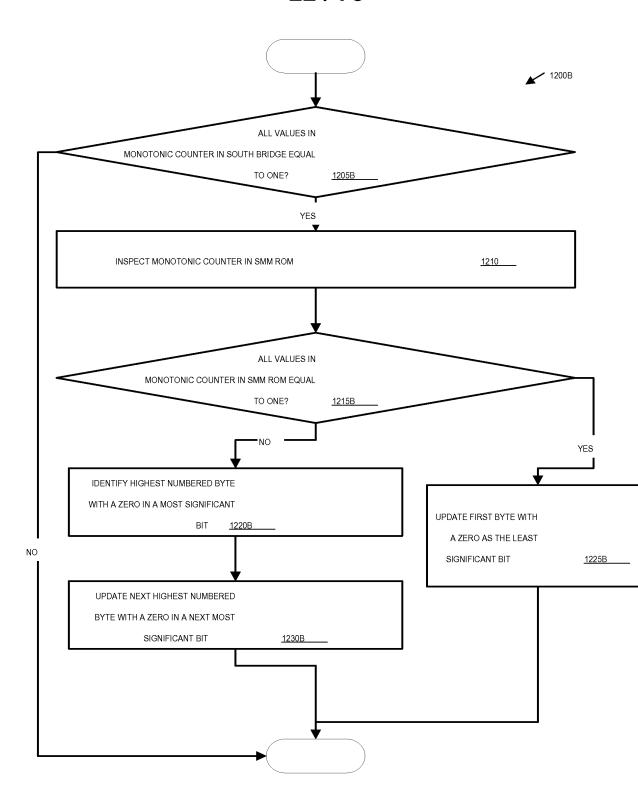
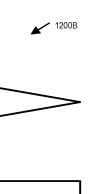
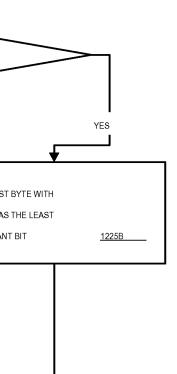


Fig. 12B



210\_\_\_



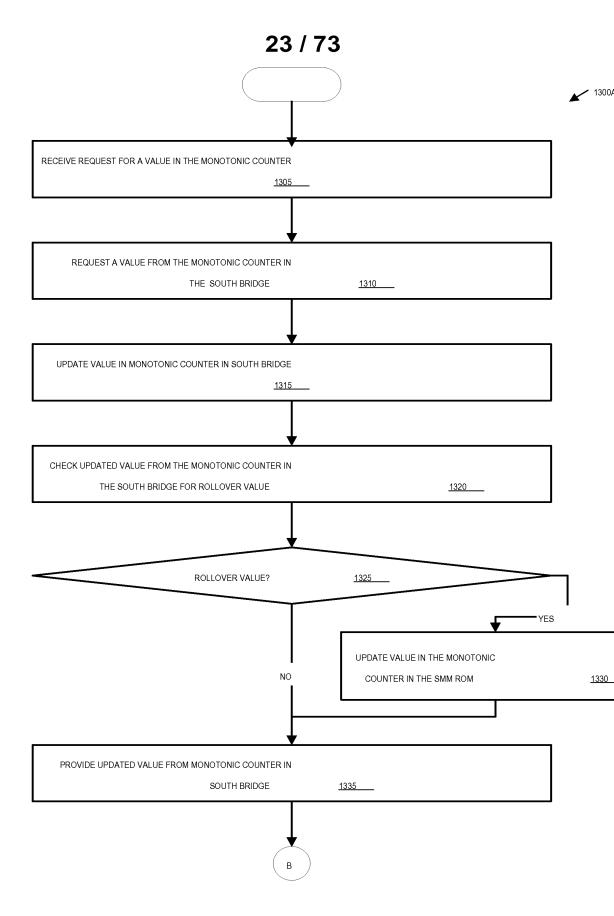
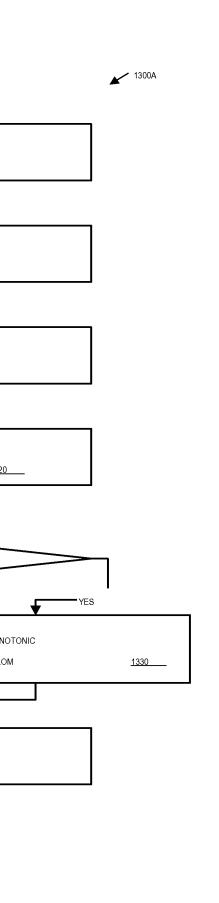
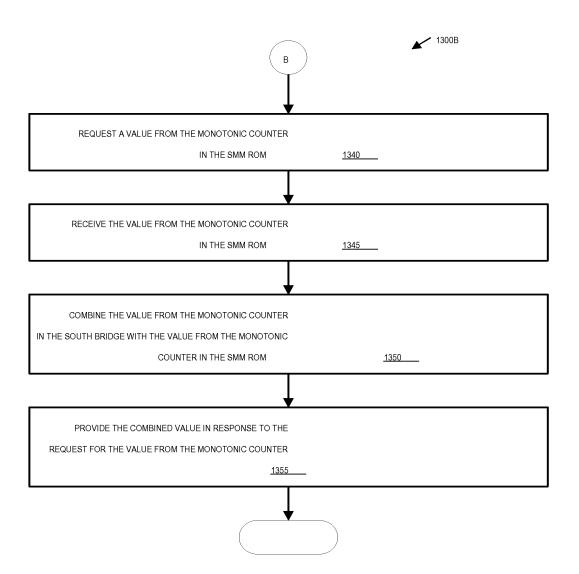
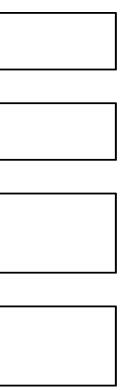


Fig. 13A







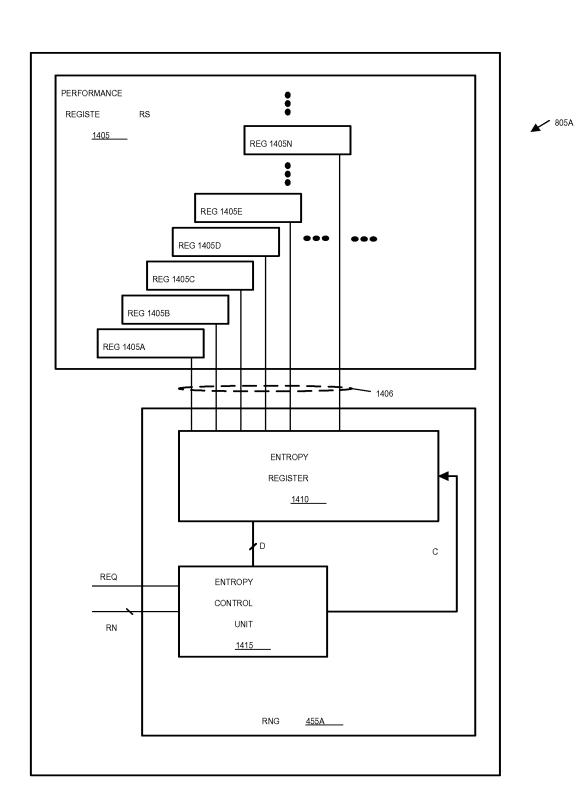
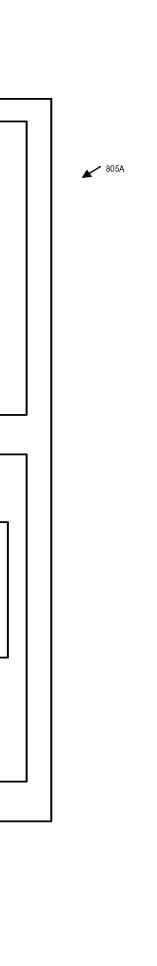


Fig. 14A



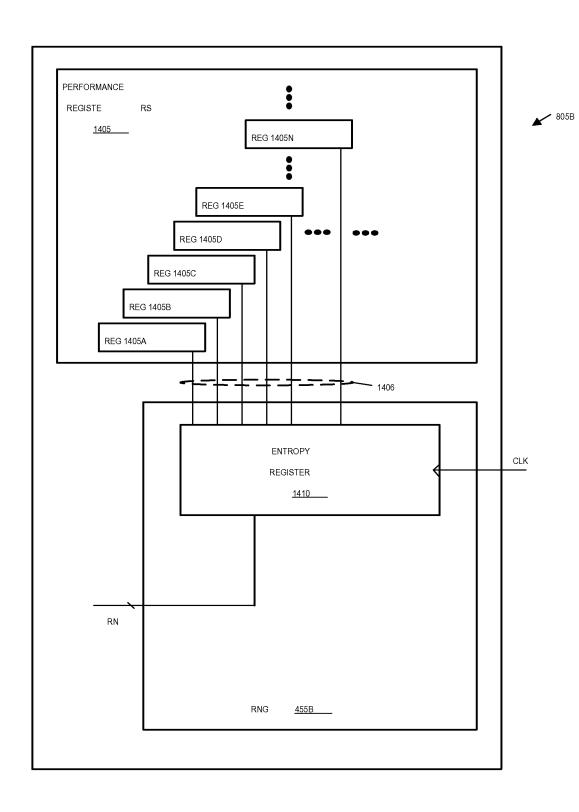
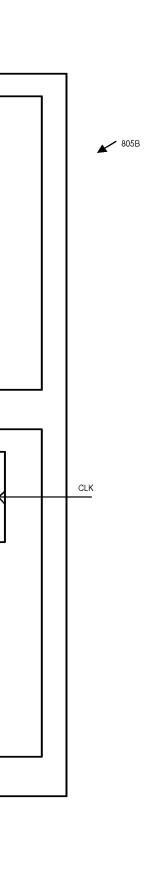


Fig. 14B



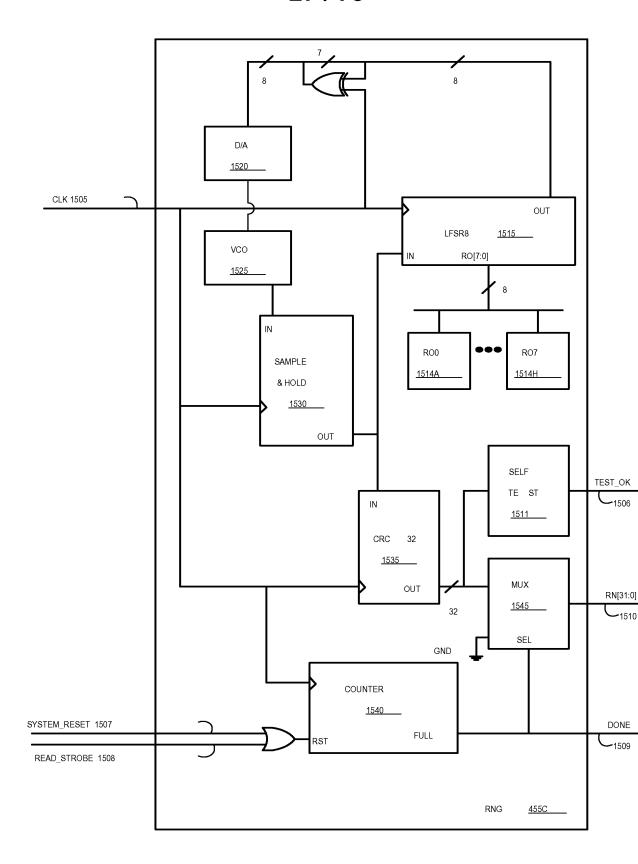
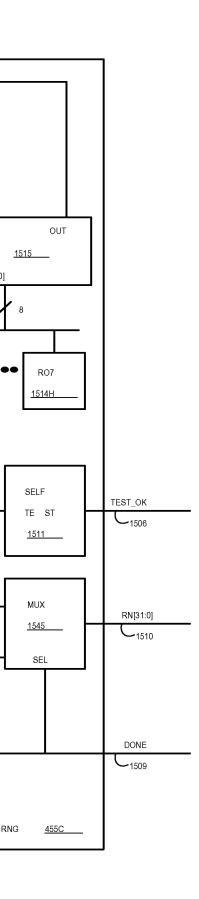


Fig. 15



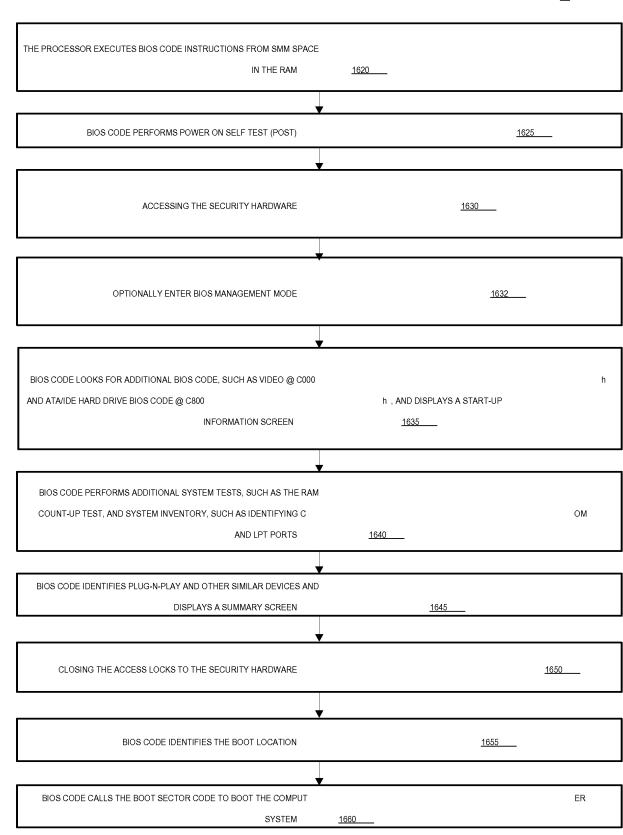


Fig. 16A

	1600A
<u>1625</u>	
30	
1632	
TART-UP	h
ОМ	
	<u> </u>
<u>1650</u>	
	_
1655	
ER	

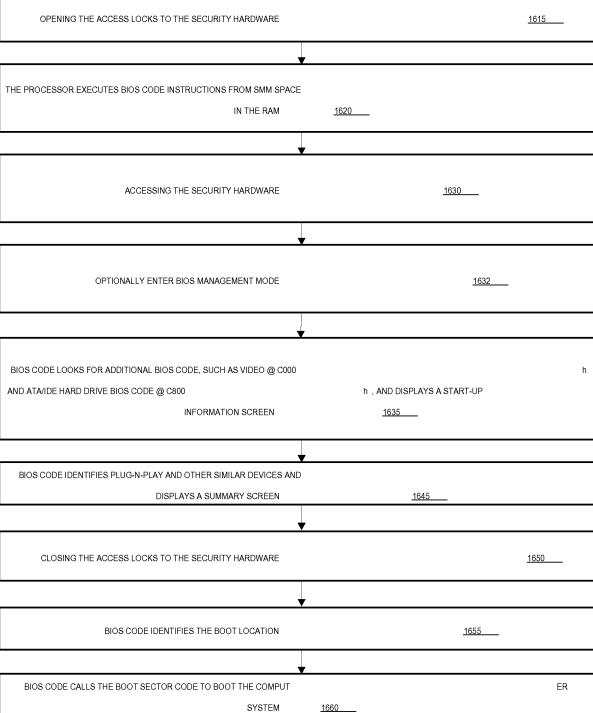


Fig. 16B

	1600B
	<u>1615</u>
<u>1630</u>	
<u>1632</u>	
A START-UP	h
_	
	<u>1650</u>
<u>1655</u>	
	ER

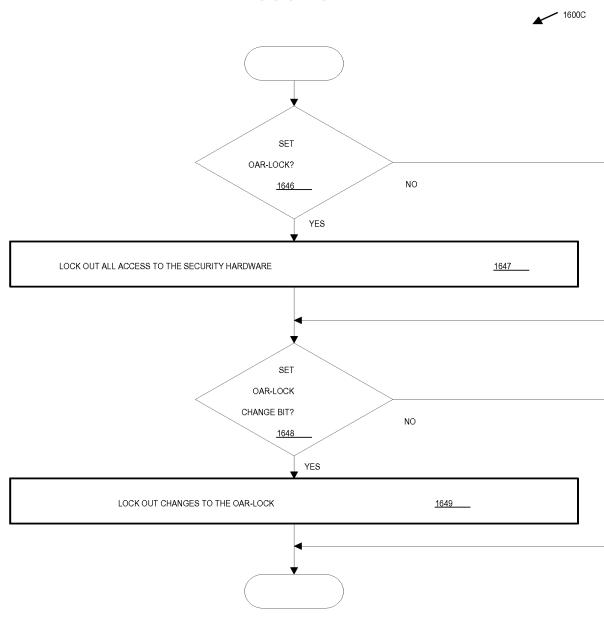


Fig. 16C



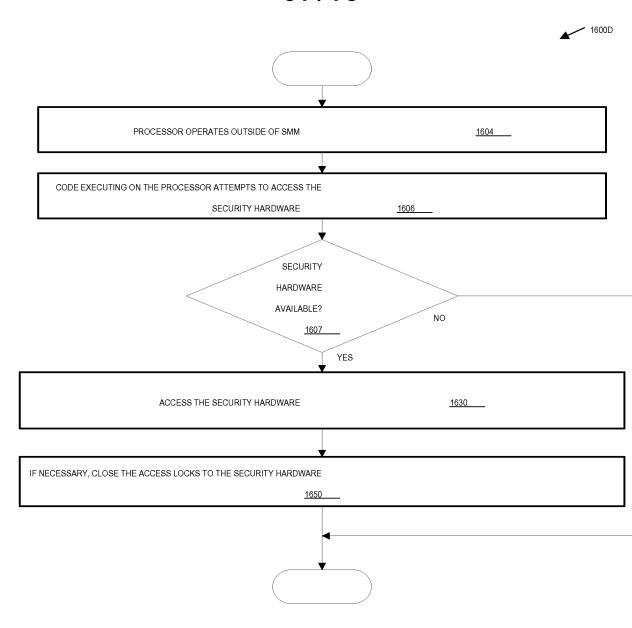


Fig. 16D

	1600D
--	-------

			_
1604			
			_
	·		

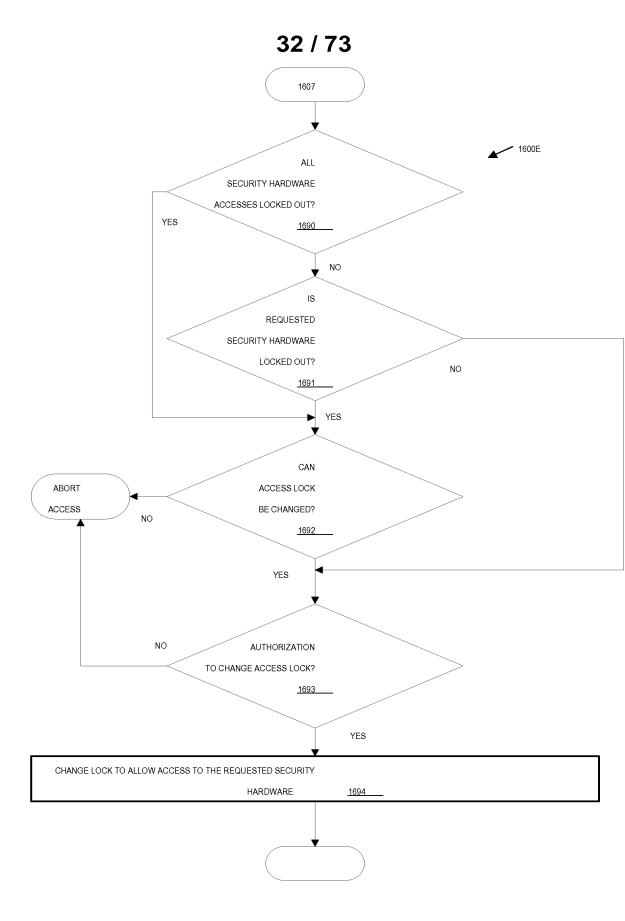
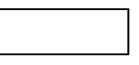


Fig. 16E







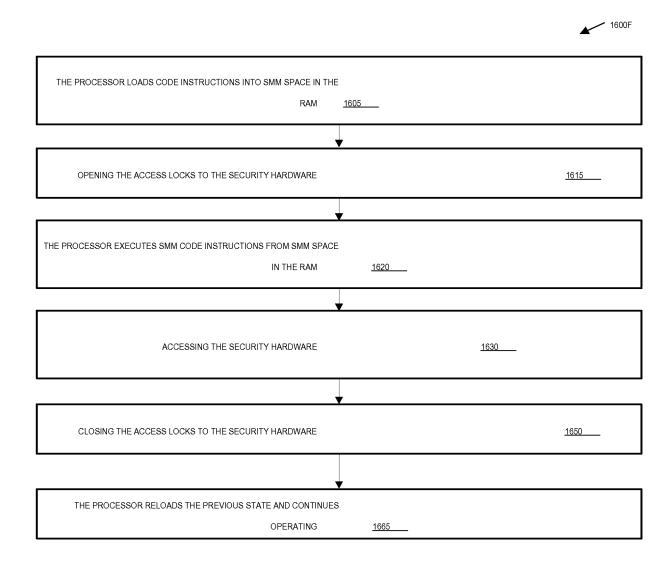


Fig. 16F

1600F	
<u>1615</u>	
_	
<u>1650</u>	

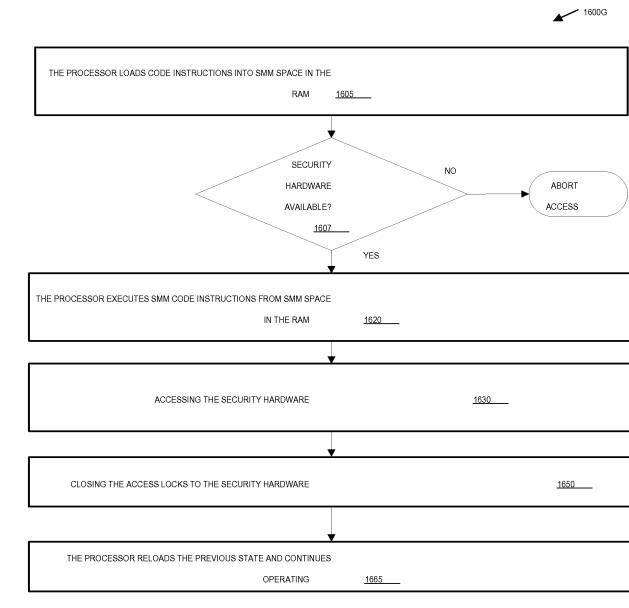


Fig. 16G

			1600G	
_	•	ABORT ACCESS		
1630				
		1650	_	

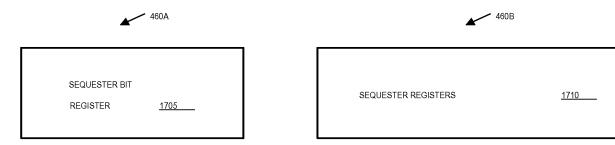
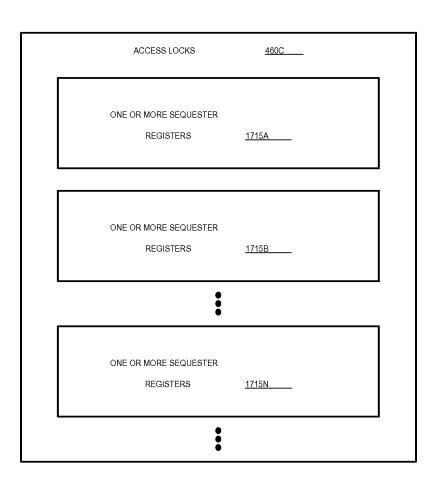


Fig. 17A Fig. 17B



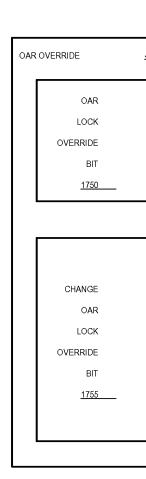
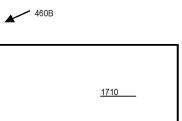


Fig. 17D



7B

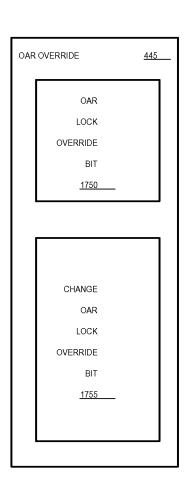


Fig. 17D

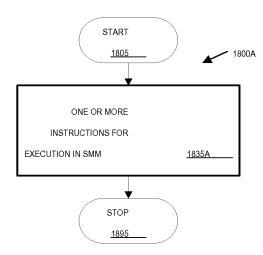


Fig. 18A

## **PRIOR ART**

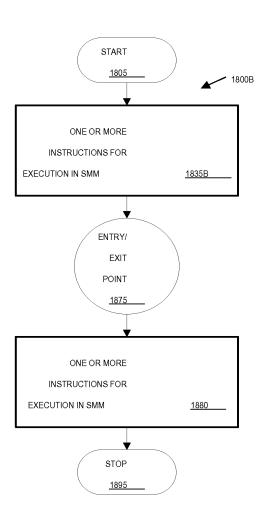
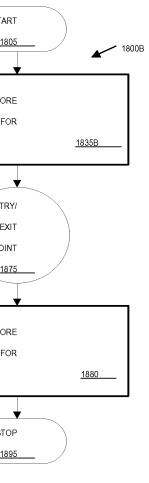


Fig. 18B





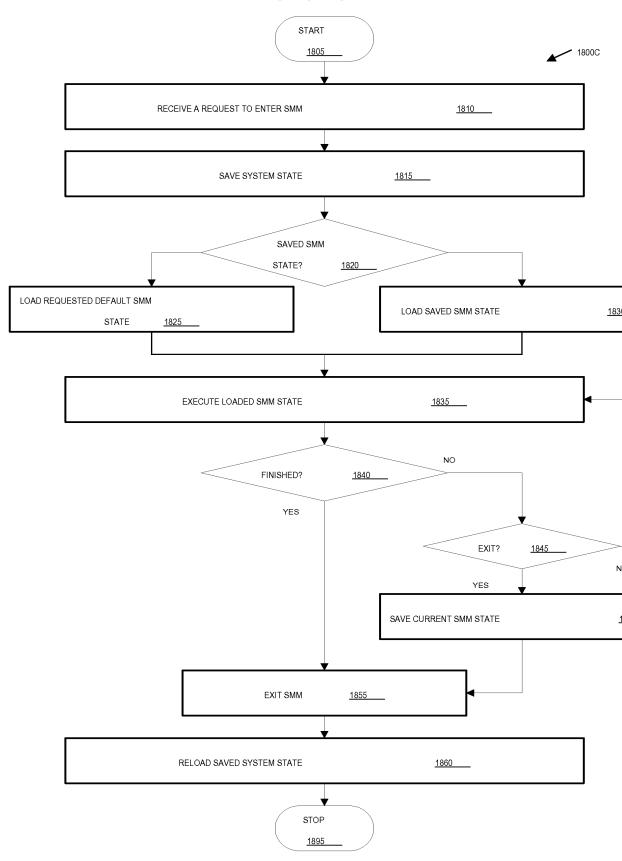


Fig. 18C

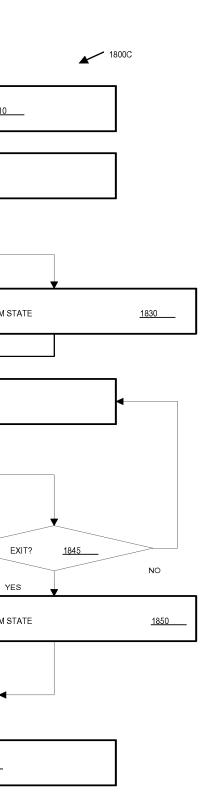


Fig. 18C

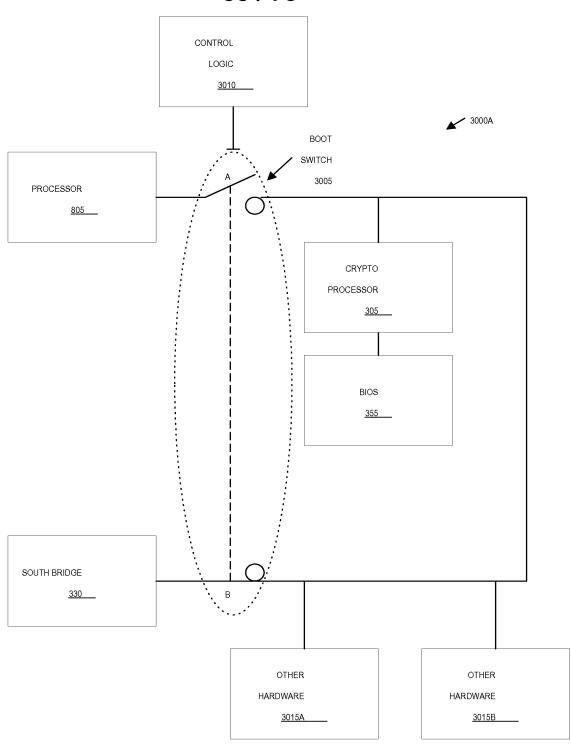
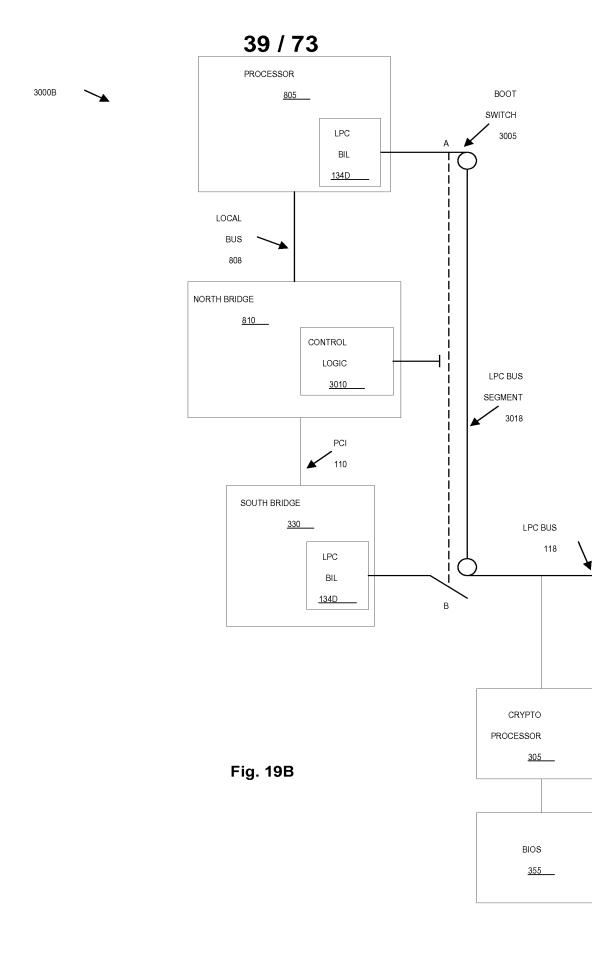
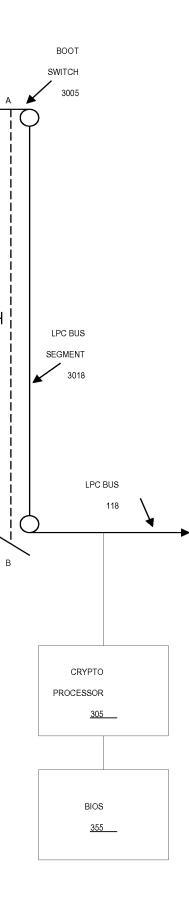


Fig. 19A



OTHER HARDWARE 3015B





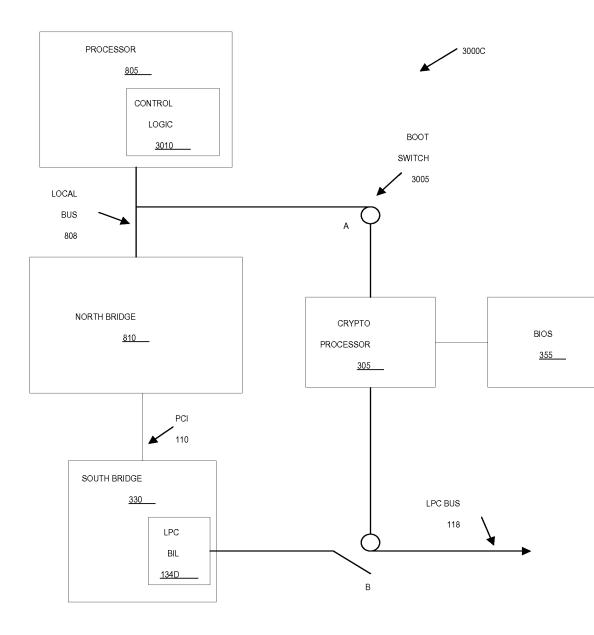


Fig. 19C



BIOS



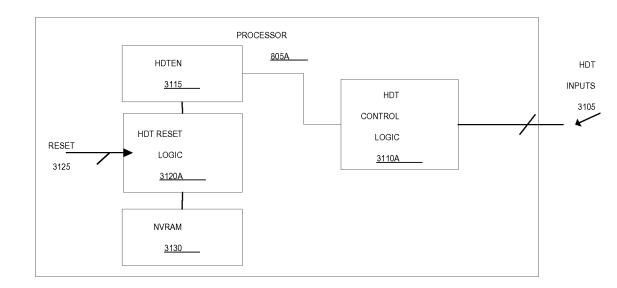


Fig. 20A

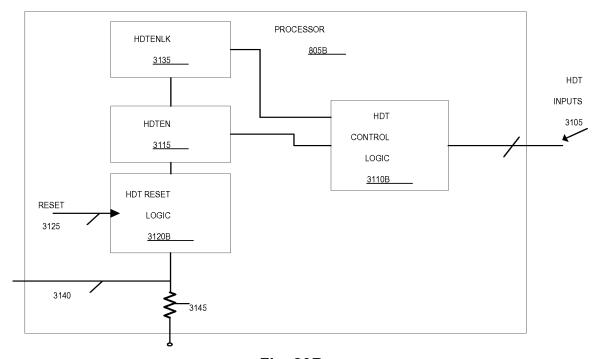
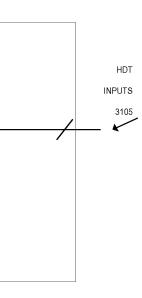
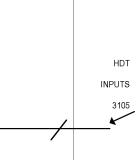
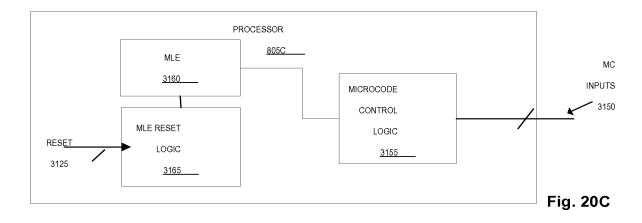
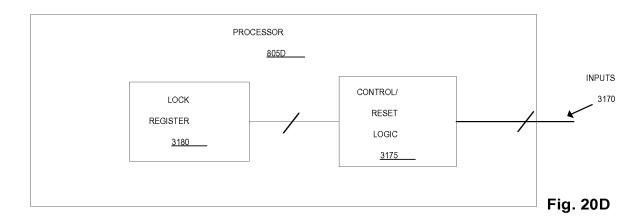


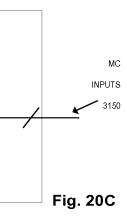
Fig. 20B

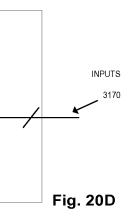












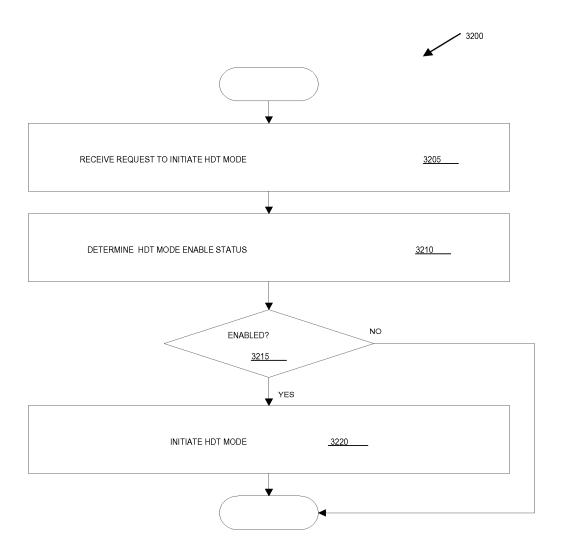


Fig. 21

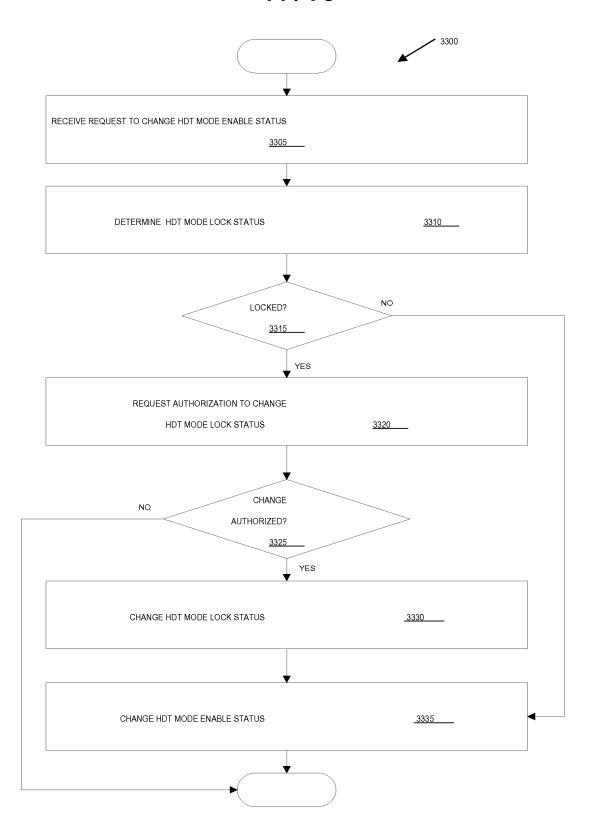


Fig. 22

0			
-			
•			

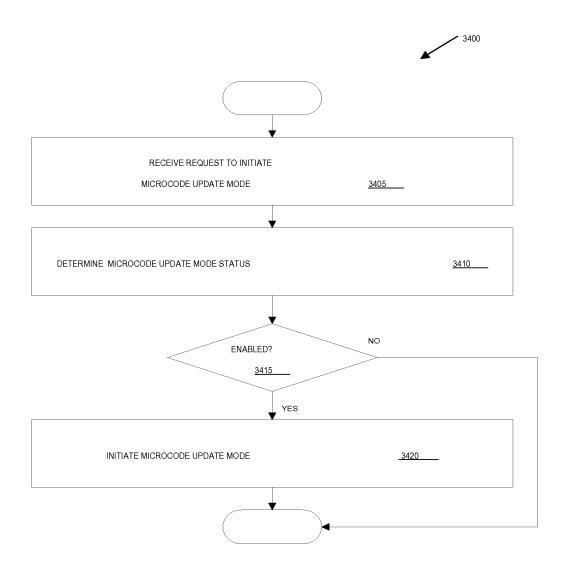


Fig. 23

\_

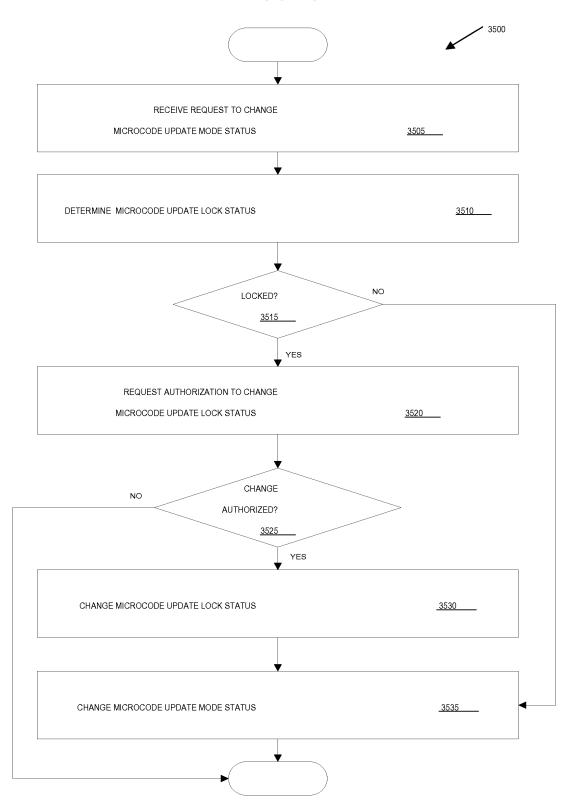


Fig. 24



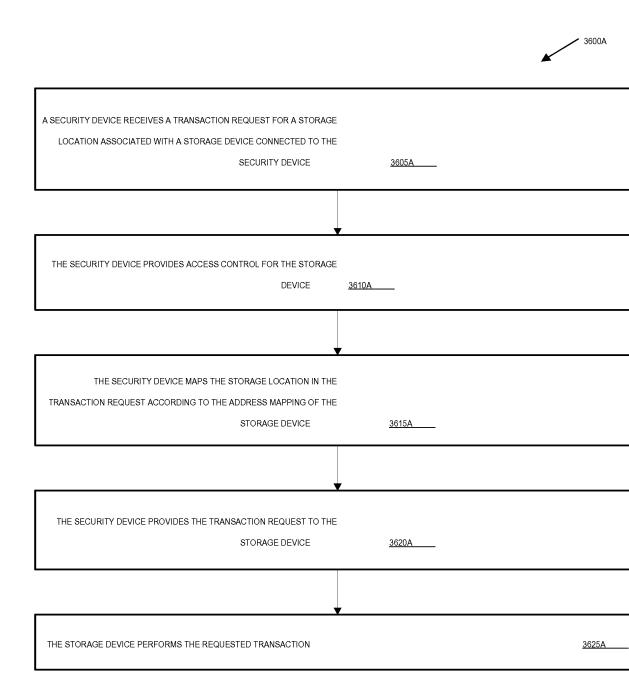
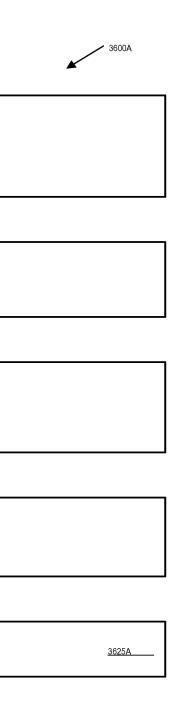


Fig. 25A



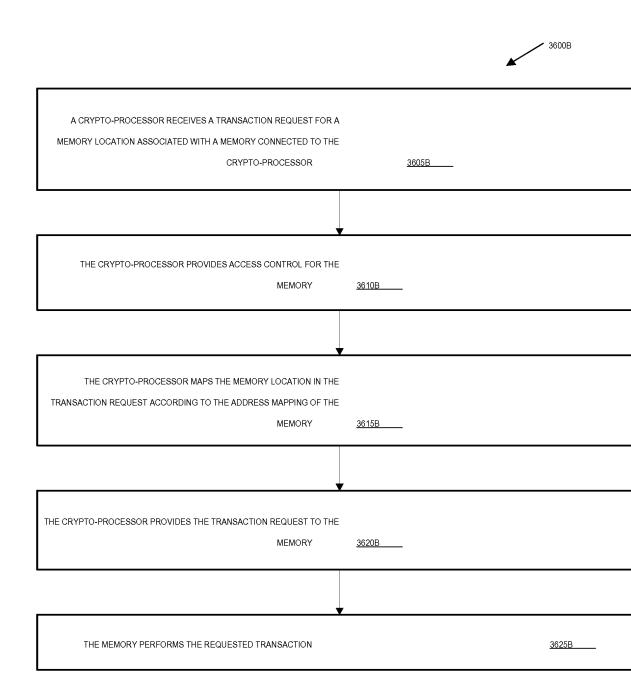
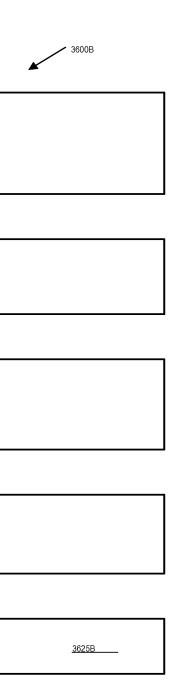


Fig. 25B



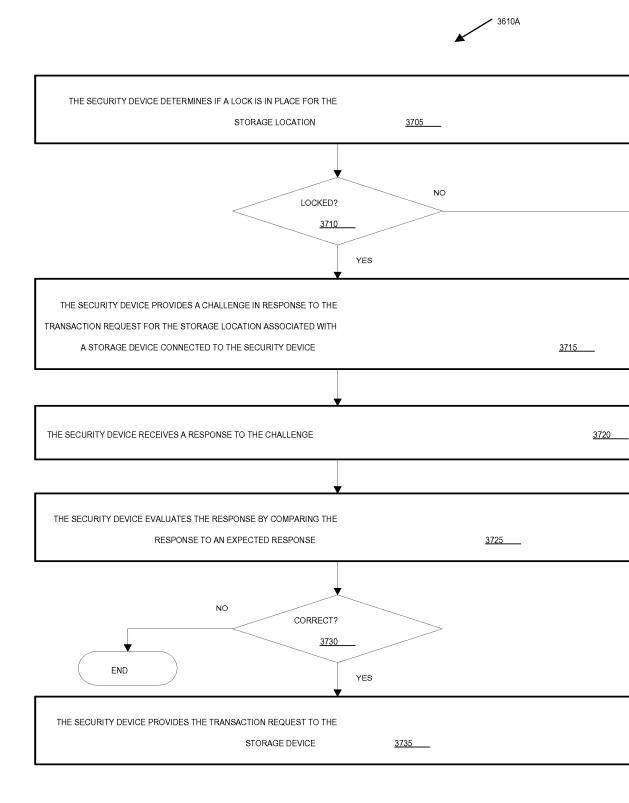


Fig. 26

3610A		
	<u>3715</u>	
	3720	_
3725		



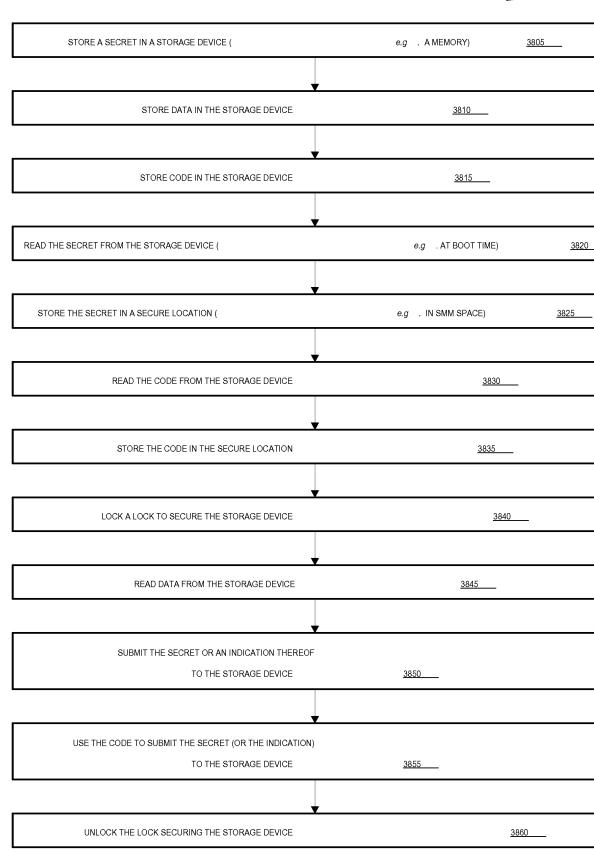


Fig. 27

×	3620
IORY)	<u>3805</u>
3810	
<u>3815</u>	
BOOT TIME)	<u>3820</u>
M SPACE)	<u>3825</u>
3830	
3835	
<u>3840</u>	_
3845	

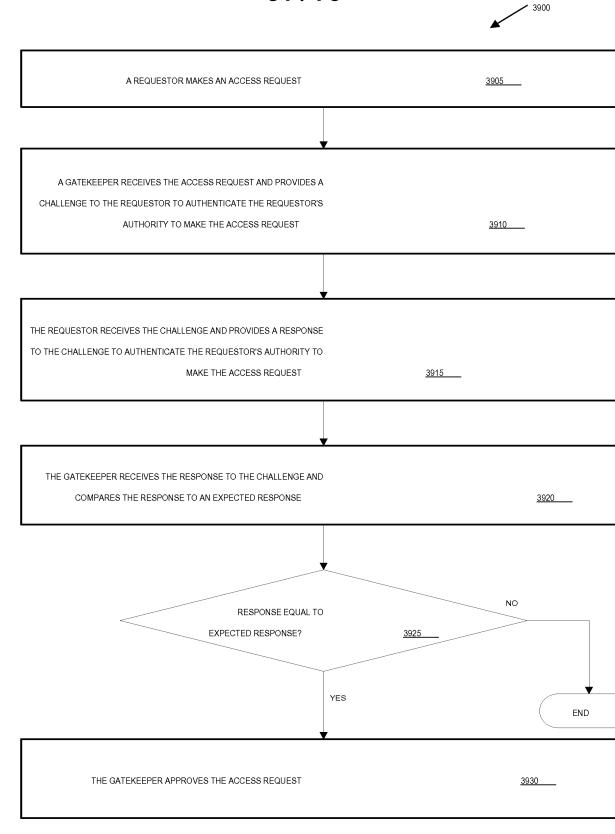
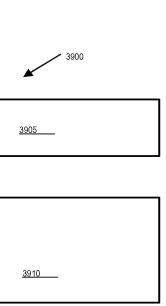
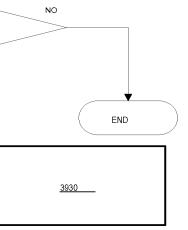
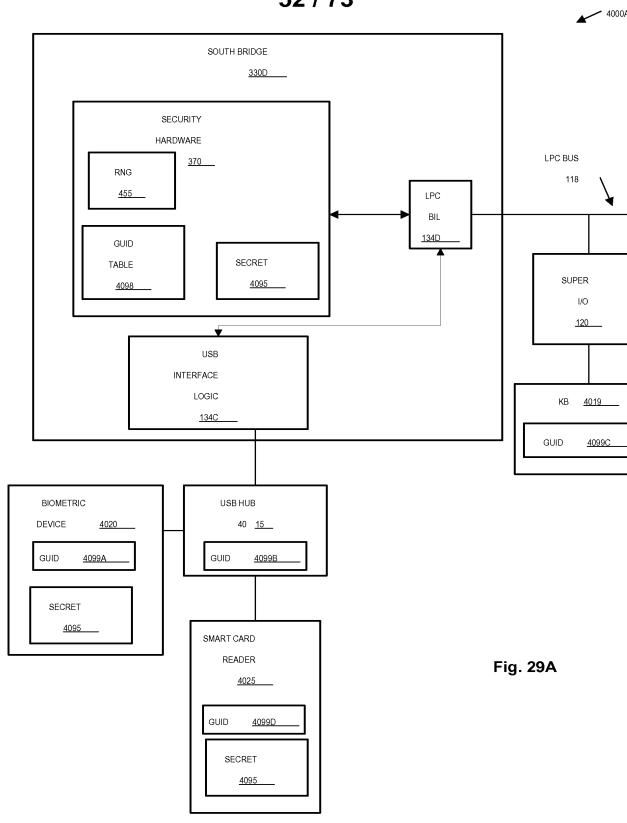


Fig. 28 (Prior Art)



<u>3920</u>\_\_\_





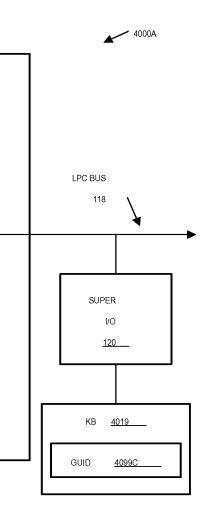
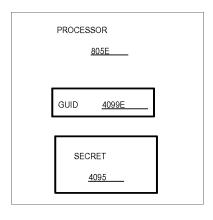


Fig. 29A



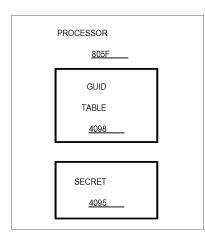
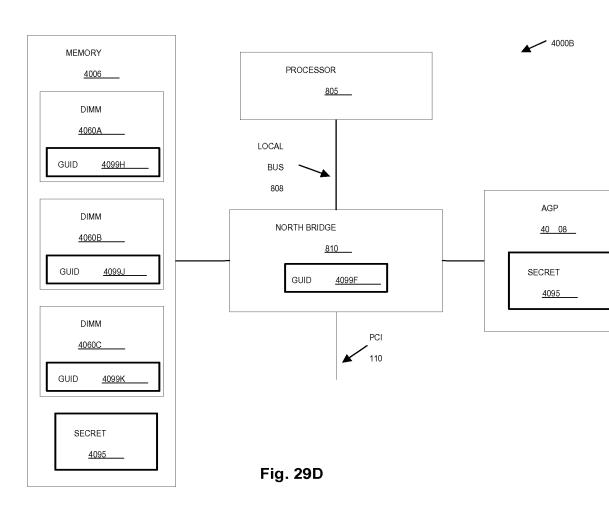


Fig. 29B Fig. 29C



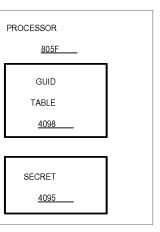
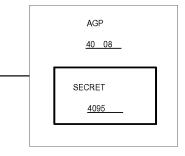
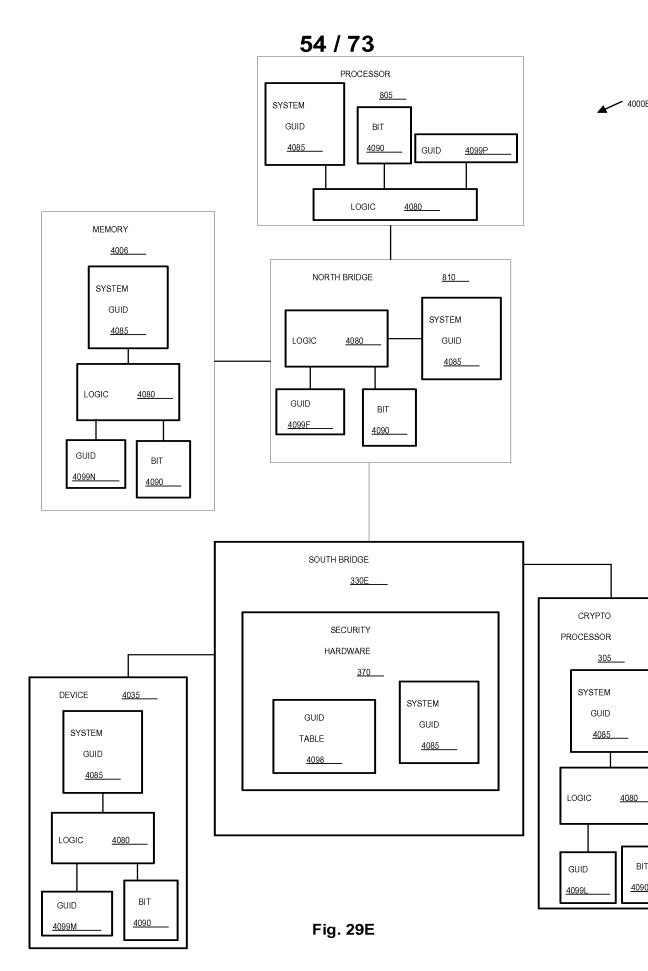
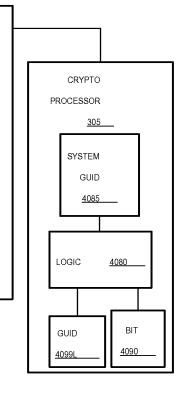


Fig. 29C











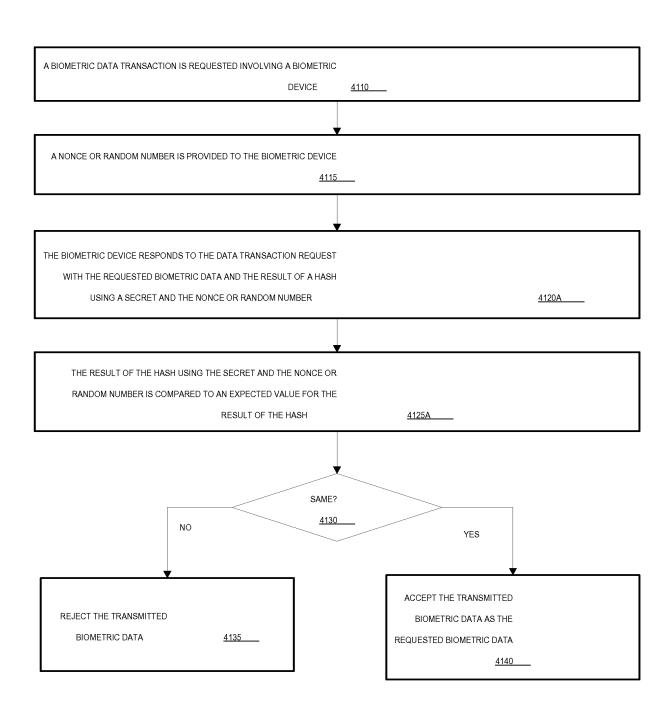
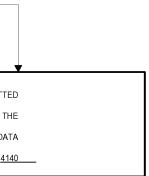


Fig. 30A



<u>4120A</u>



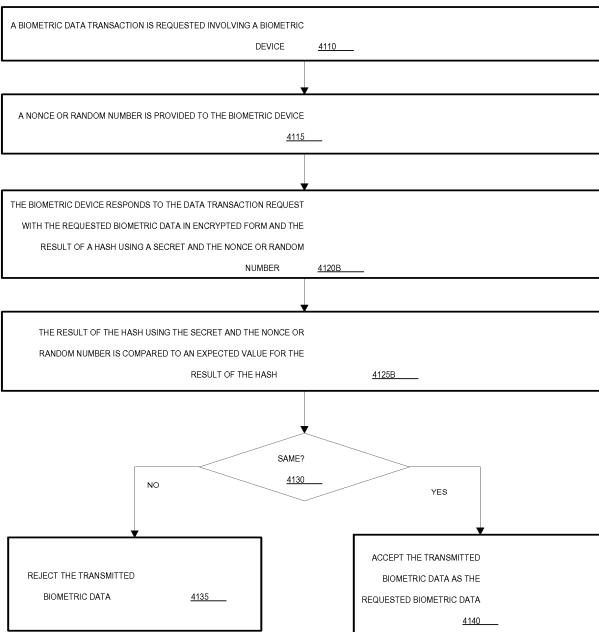
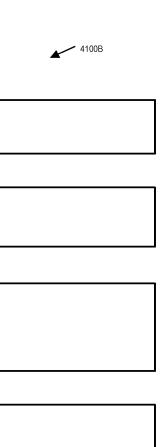


Fig. 30B



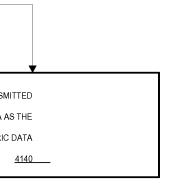


Fig. 31A

DATA

4235

DATA OR SEND THE DATA

4240A

	4200A
<u>4210</u>	
<u>4215</u>	

ESETED
HE DATA

4240A

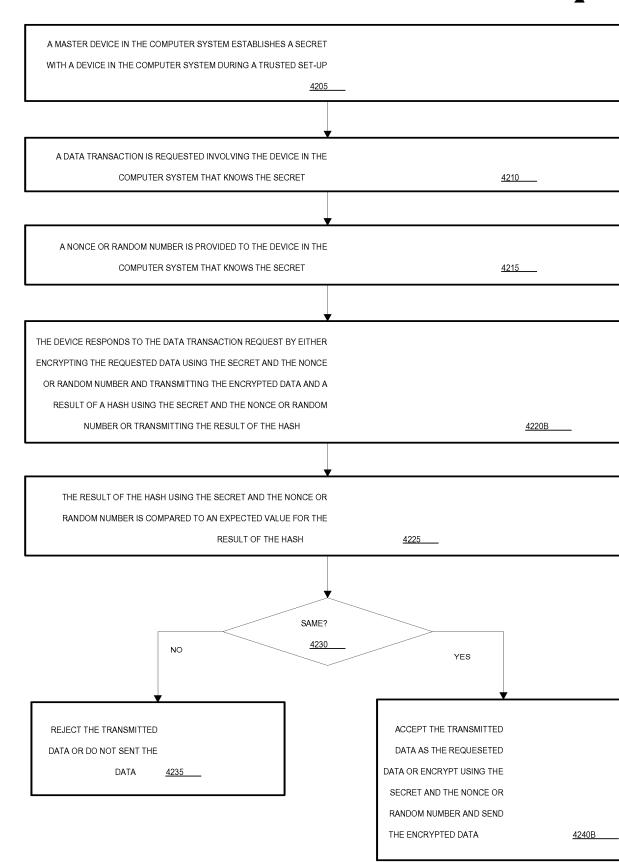
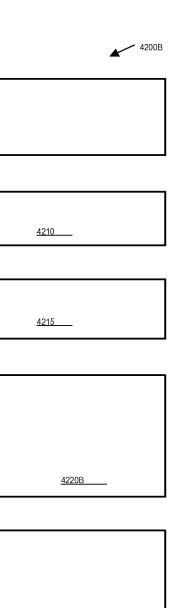
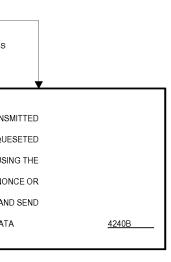


Fig. 31B





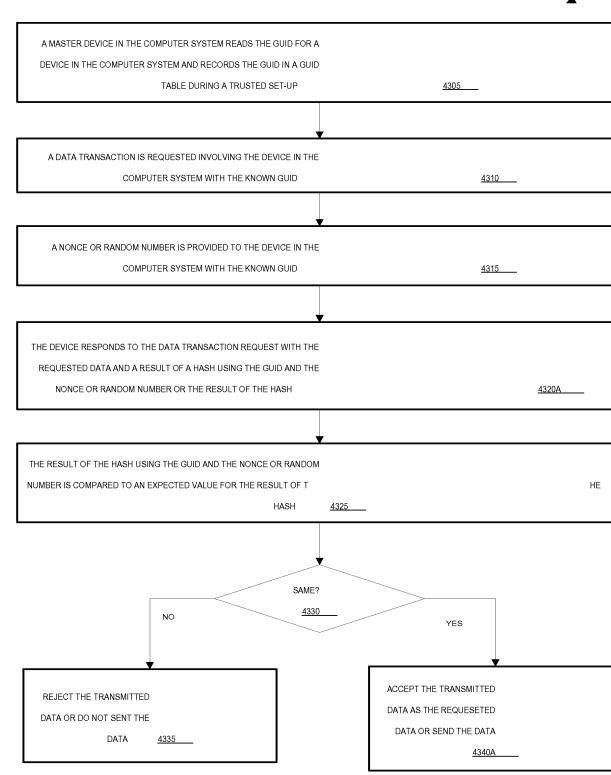


Fig. 32A

	4		4300A
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4310			
4315			
	4320A		
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NSMITTED
RUESETED
THE DATA
4340A

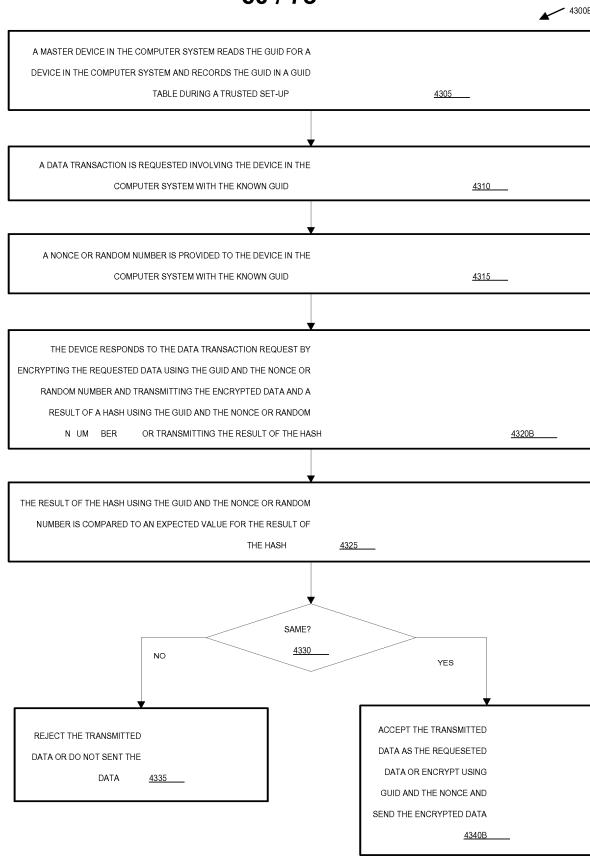
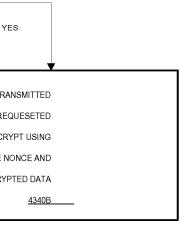
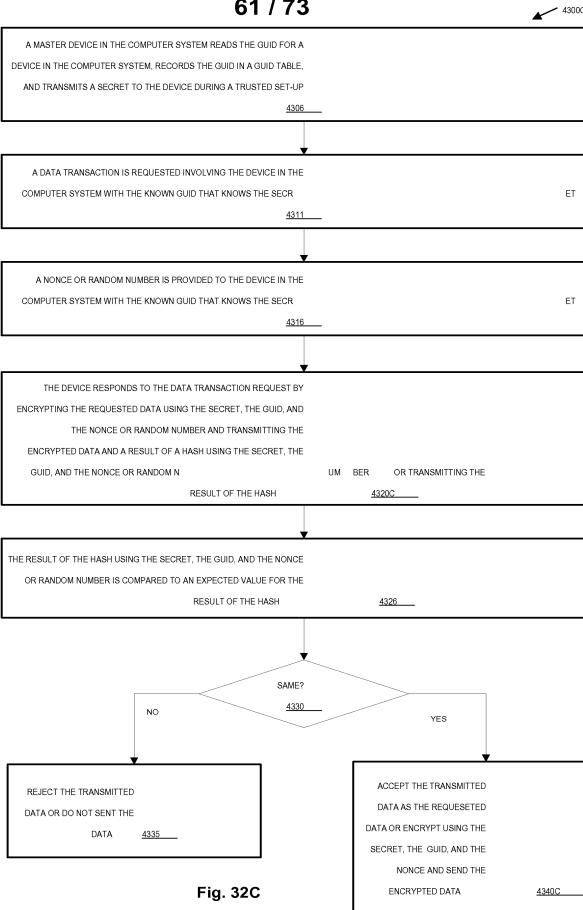


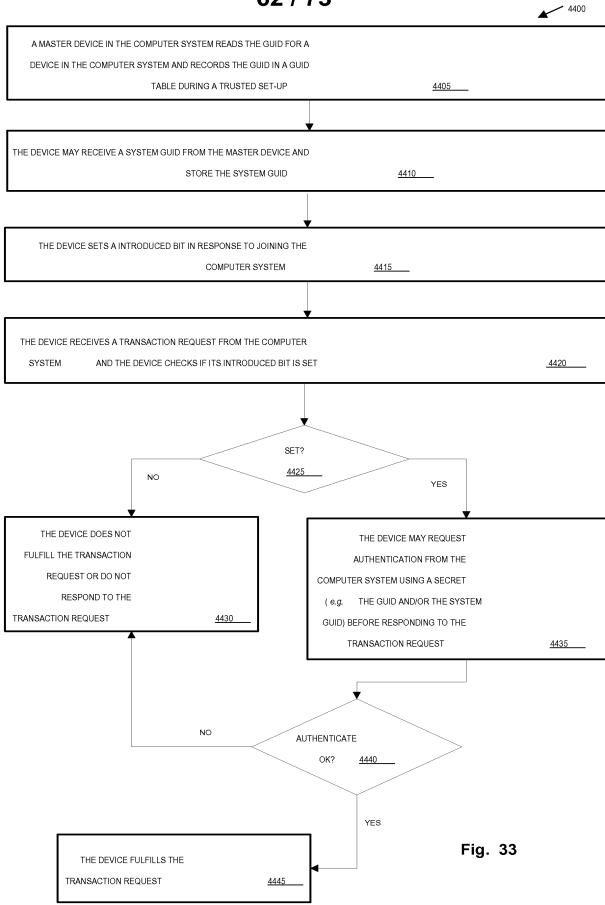
Fig. 32B

			4300B	
305	-			
	<u>4310</u>	_		
				_
	<u>4315</u>			
	1010	_		
		4320B		
				_









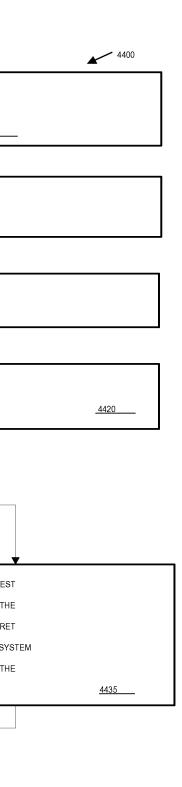


Fig. 33

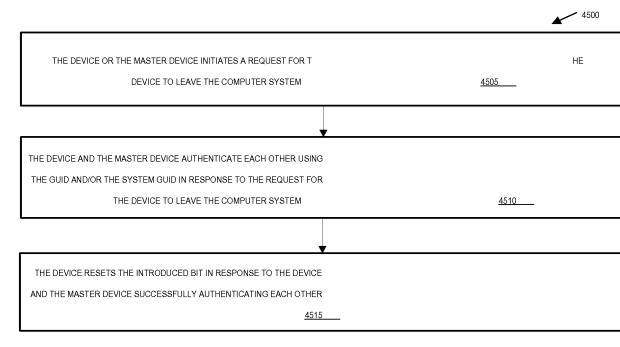


Fig. 34

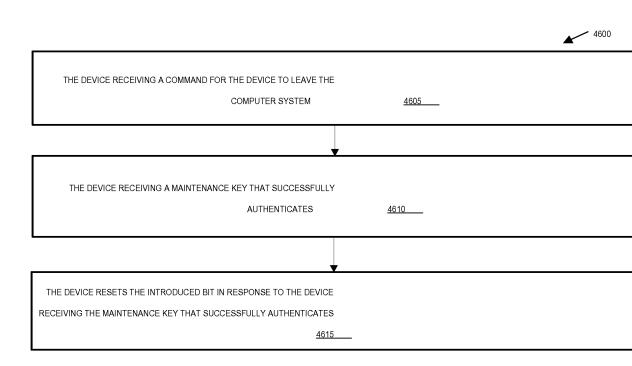
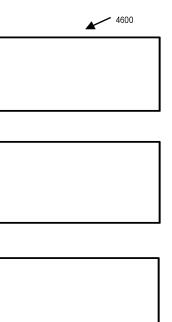
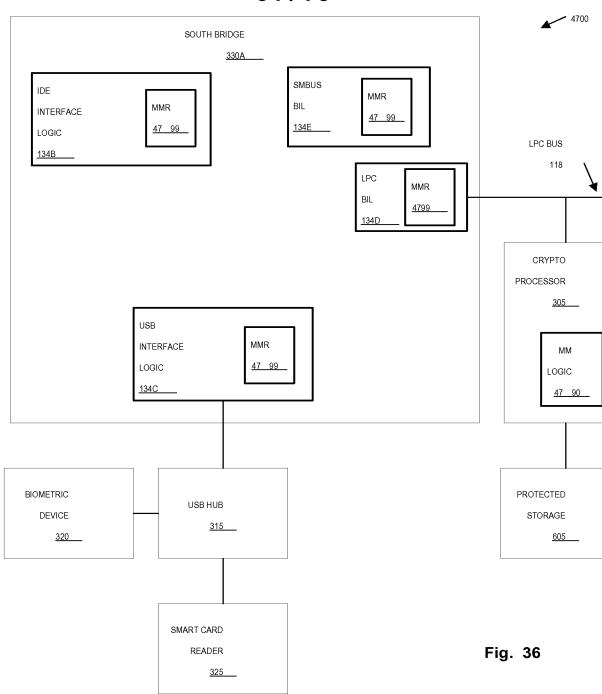


Fig. 35

	4500
	HE
<u>4505</u>	
<u>4510</u>	





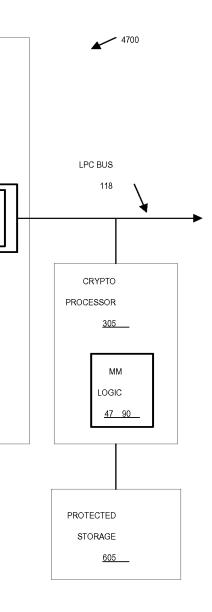


Fig. 36

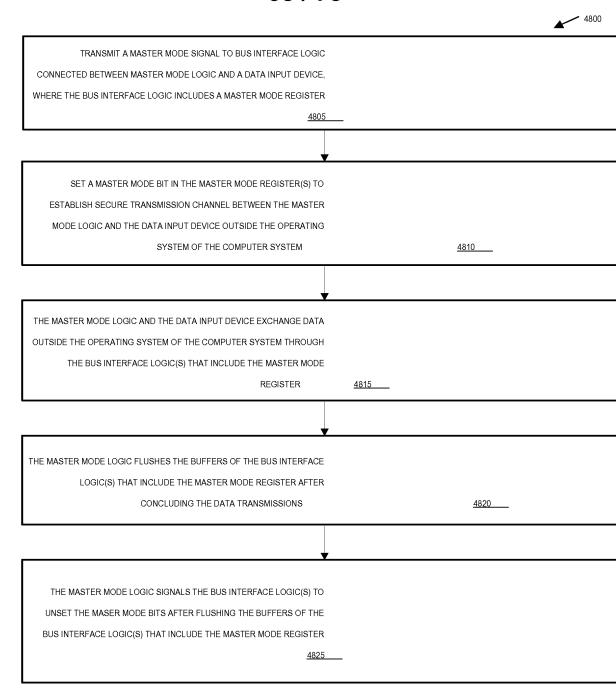


Fig. 37

	4800
810	
<u>4820</u>	

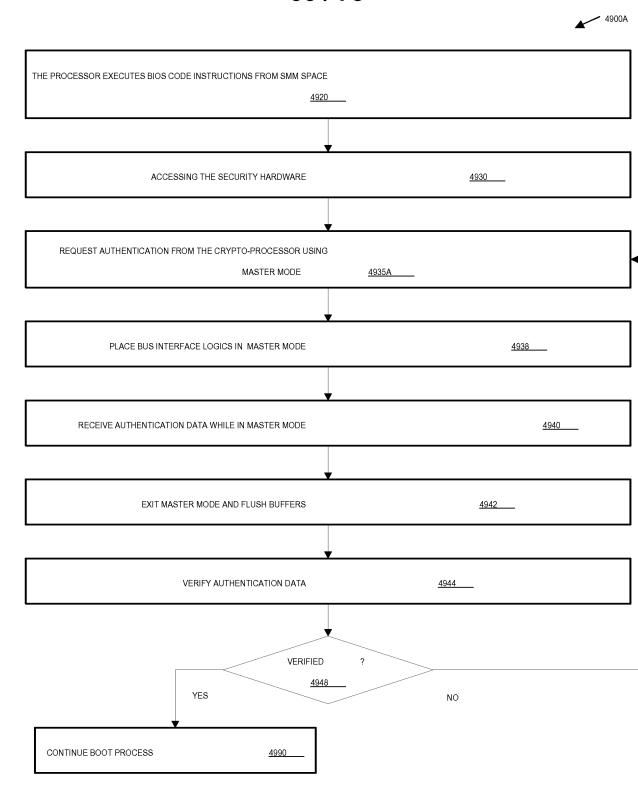


Fig. 3 8A

4900A	
0	
	•
	,
4938	
<u>4940</u>	
942	

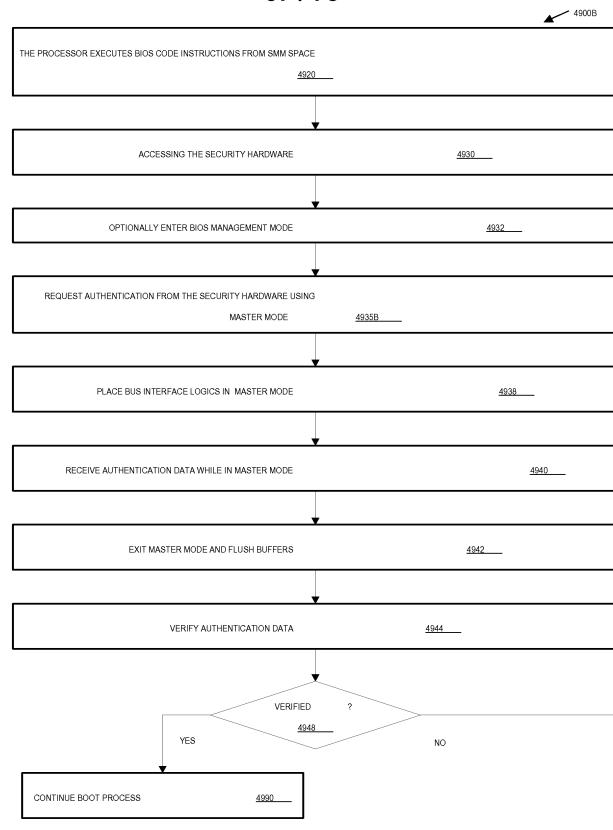


Fig. 3 8B

4900B	
4930	
	1
4932	
	1
	<b>←</b>
<u>4938</u>	
	ì
<u>4940</u>	
	1
4942	
	1
-	

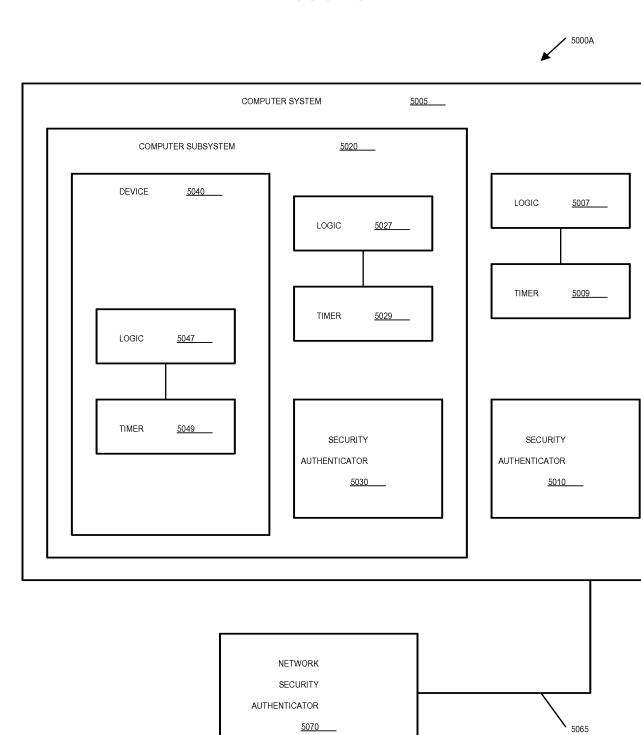
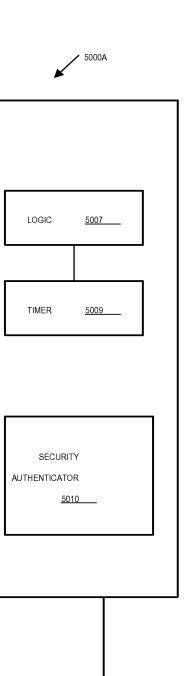
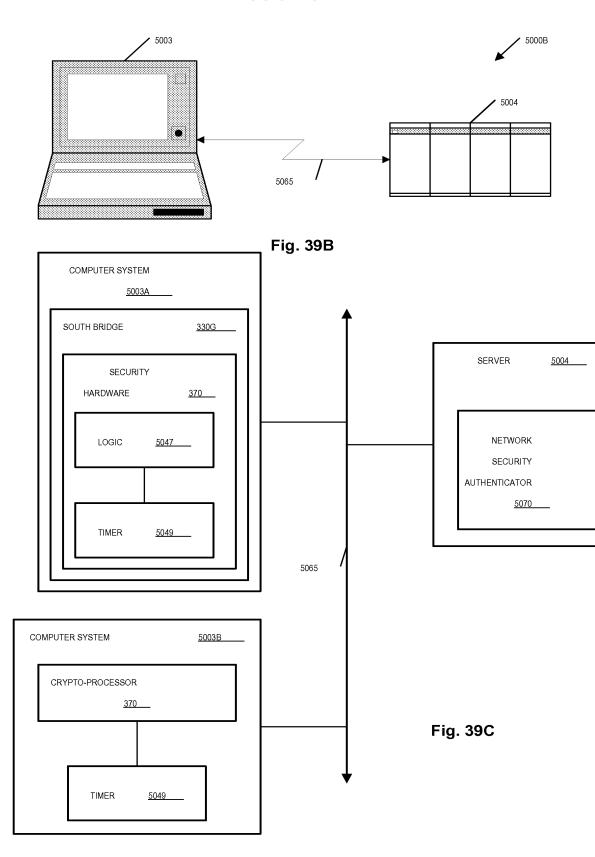
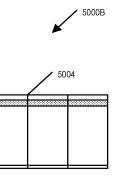
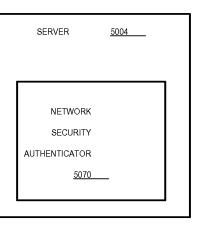


Fig. 39A

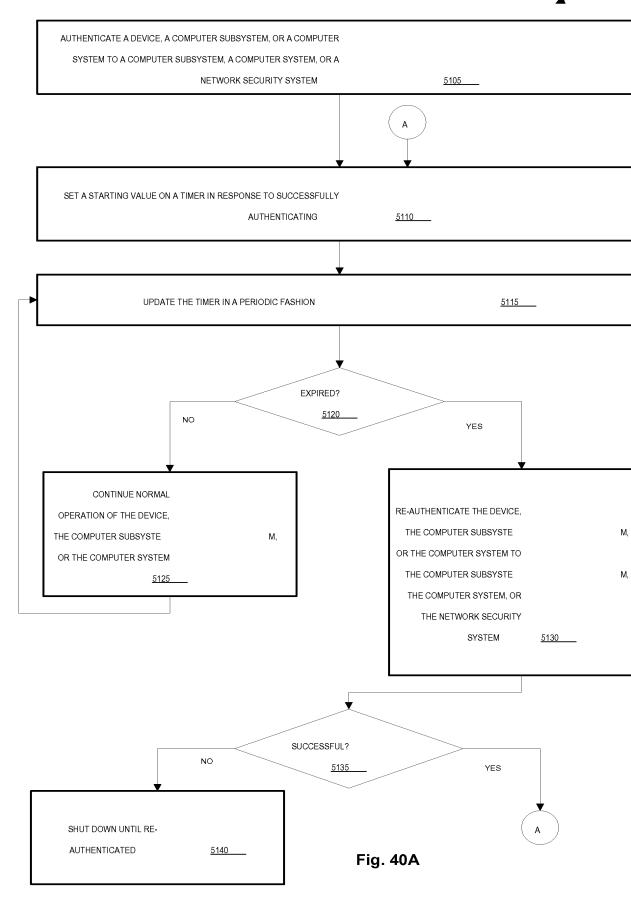


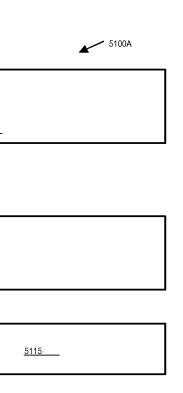


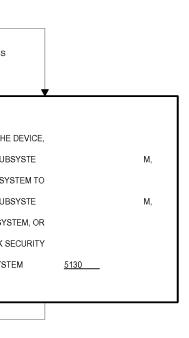


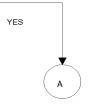


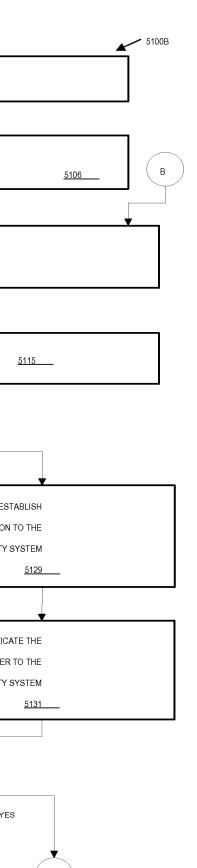
ig. 39C











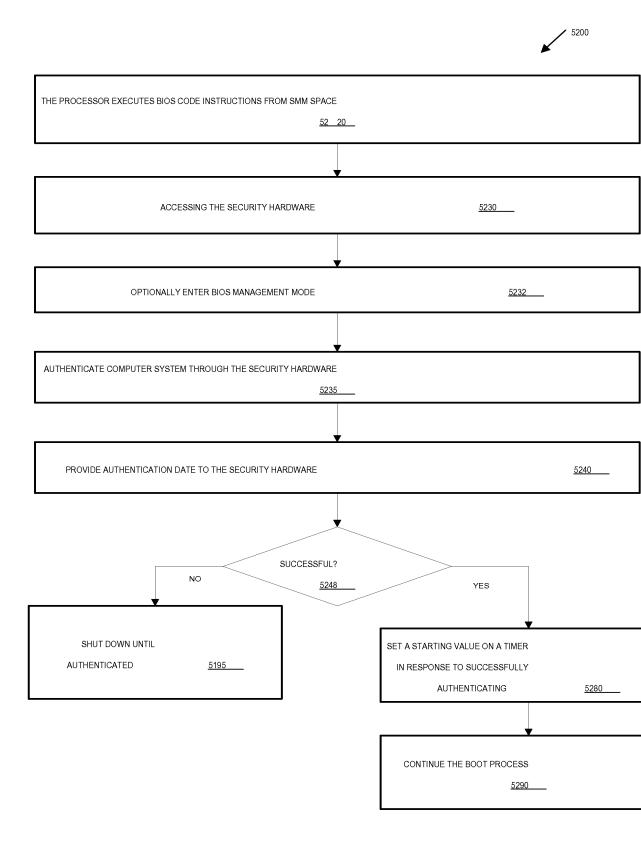
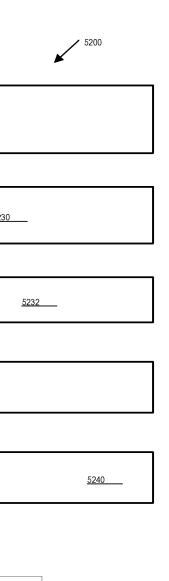
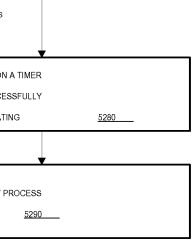


Fig. 41





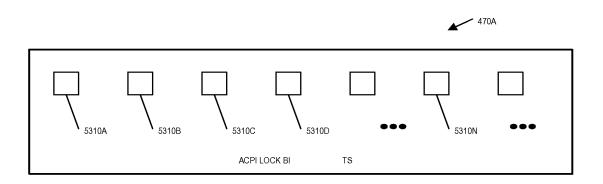


Fig. 42A

SECURE SYSTEM MANAGEMENT REGISTERS  470B		
ACPI RANGE REGISTERS	<u>5320</u>	
ACPI RULE REGISTERS	5330	



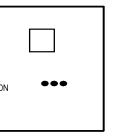


Fig. 42A

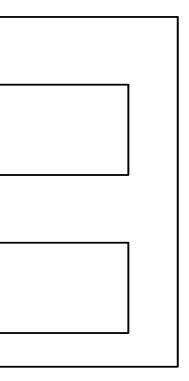


Fig. 42B